

### 1 General Description

The NB1043AP is a reference design that can be used as an example to develop a self-contained GPS receiver module based on the Nemerix NJ1030A and NJ1006A GPS chipset. The receiver includes a passive patch antenna and the flash memory necessary to store the Nemerix NS1030 GPS firmware. It is built with 0.8mm pitch BGA devices in order to allow for lower cost PCB assembly techniques.

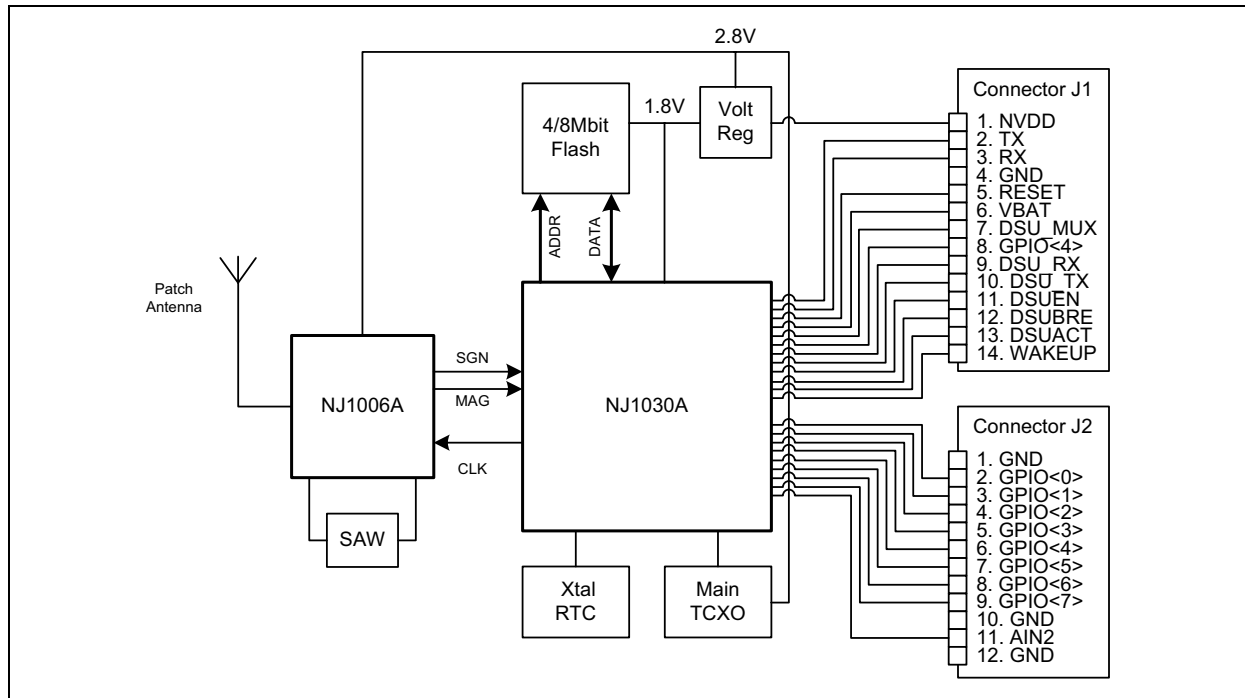
The NB1043AP interfaces to the host system via the NJ1030A UART using the NMEA protocol expanded with Nemerix specific commands. It requires a 3.3V main power supply and a back-up voltage of 1.2V to 2V to maintain relevant GPS and system information in the non volatile portion of the NJ1030A memory.

The NB1043AP is delivered with a 4MBit Flash device and a 32.734MHz TCXO. Other configurations are possible.

### 1.1 Features

- GPS receiver module with passive patch antenna
- Based on NJ1030A and NJ1006A chipset
- Low power consumption: 19mA fully active
- Compact design: 25.9x28.9x7.5mm
- SMT compliant
- Simple UART interface
- BGA 0.8mm pitch components
- Support of WAAS/EGNOS (SW option)
- Support of 4MBit and 8MBit flash
- Support of 16.367MHz and 32.734MHz TCXO

Figure 1. NB1043AP Block diagram



## 1.2 Specifications

Parameter	Min	Typical	Max
Supply Voltage on (NVDD) pin	3V	3.3V	6V
Back up power supply voltage (VBAT)	1.2V		2V
Operating Temperature	-30°C		+65°C
Power Consumption in acquisition (fully active)		23mA	
Power Consumption in tracking (fully active)		19mA	
GPS Channels		16	
Tracking sensitivity	-150dBm		
TTFF Cold Start @ -135 dBm		46 sec	
TTFF Warm Start @ -141 dBm		34 sec	
TTFF Hot Start @ -141 dBm		5 sec	
Re-acquisition time @ -147 dBm		< 3 sec	
Update rate		1 Hz	

Frequency	1575.42MHz - L1 C/A Code
I/O Port	UART interface
Protocol	NMEA (Extended)
Weight	12g (with 25x25x4 mm patch antenna)
Mating Connector	14 pin and 12 pin 1.27mm pitch headers
Dimensions	25.9x28.9x3.5 mm (without antenna)

## 2 Communication Protocol

The communication protocol is the standard NMEA expanded with Nemerix commands.

## 3 NB1043AP Receiver Parts

### 3.1 Antenna

The antenna is a passive patch antenna of 25x25mm. The antenna is mounted on one side of the NB1043AP, while all the other components are mounted on the other side. To improve antenna performance, a dedicated ground plane may be inserted between the antenna and the board. Ground plane and NB1043AP can be attached together with double sided adhesive tape. In case a strong electrical connection is needed between grounds, a conductive tape or a hole in the tape together with a conductive paste may be used.

### 3.2 NJ1006A front end

The NJ1006A is the down-converter (see related datasheet). Power supply for the NJ1006A is set to 2.8V (AVDD) with a low dropout regulator. To reduce overall size, the Toyocom QQS-949FA 2x2.5x1mm L1 SAW filter is used.

The NJ1006A has a single stage cascode integrated LNA with 20dB gain and 1.5dB NF used for best sensitivity. The LNA is noise matched.

### 3.3 NJ1030A base-band

The GPS base-band processor is the NJ1030A. It is used in its minimum configuration, i.e. only as GPS processor (see related datasheet). The only required external part is the flash memory storing the NS1030 GPS firmware. Power supply is set to 1.8V (DVDD) with a linear regulator. Supply voltage for the core is set to 1.2V using the on-chip regulator. Communication to the NJ1030A is provided via the UART.

### 3.4 Flash Memory

A 4Mbit (8Mbit) organized in 256k (512k) x 16bit flash memory is needed by the NJ1030A IC. SST39WF400A (SST39WF800A) is an adequate flash for this application. It operates from DVDD and comes in a 6x8mm BGA package.

A different flash memory type can be used, as long as it is pin compatible with the memories described here. The voltage supply must be in the NJ1030A DVDD specification (1.8V-3.3V) and the DVDD voltage regulator (part U2) must be changed accordingly.

**Note:** the NB1043AP is delivered with 4Mbit SST flash device as default configuration. Any change of the flash configuration may require a different flash programmer configuration (refer to the flash programmer documentation). Flash memory access time shall be 90 ns or lower.

### 3.5 Clock

The clock frequency is set to 32.734MHz and is generated by a TCXO. The chosen TCXO is the Rakon IT5325B. It has 2.0ppm accuracy over temperature, a size of 5x3.2x1.5mm and requires a minimum voltage supply of 2.7V. The TCXO is sensitive to power supply noise, therefore the AVDD power supply of the RF front-end is used. The use of a 16.367 MHz TCXO is also possible in the design, if the WAAS/EGNOS functionality is not enabled in the GPS software.

**Note:** the NB1043AP is delivered with 32.734MHz TCXO as default configuration. If a 16.367MHz TCXO is used, a different NS1030 SW build is necessary. Also the configuration of the flash programmer must be adapted accordingly (see dedicated documentation).

### 3.6 RTC and Battery Backup

The NJ1030A includes a real time clock and 8kB NVRAM. This allows time and navigation database to be maintained when the NB1043AP is powered down. The RTC crystal is a tuning fork type, 32.768kHz crystal. A Microcrystal MS3V-T1R in a 1.45(w)x6.7(l)x1.45(h)mm package is the selected crystal.

RTC and NVRAM require a supply voltage of 1.2V to 2V. Power must be provided via VBAT pin on the interface connector. Any 1.2-1.5V battery or a super-capacitor can be used. If a rechargeable battery or a super-capacitor are used, a charge circuit must be provided. This may consist of a simple resistor-diode circuit. A mean to limit charge voltage below 2V should be included if the battery can be removed while the main power is on.

A suitable battery is the Varta V15H NiMH 1.2V rechargeable battery. This battery has a capacity of 15mAh and a size of 11.5mm(diameter)x3mm(h). It can be recharged at 1.8mA via a simple diode-resistor network. If the back-up voltage is not present RTC and NVRAM do not work. As a consequence the receiver will always execute a cold start when activated.

### 3.7 Voltage Regulator

Two separate voltage regulators generated the required power supplies (AVDD and DVDD) from the main voltage supply (NVDD). AVDD is 2.8V and provides voltage to the NJ1006A and the TCXO. DVDD is 1.8V and provides voltage to the NJ1030A and the flash memory. Power for the NJ1030A core is obtained with the internal voltage regulator and it is set to 1.2V.

## 4 Interface Ports

Communication to the NB1043AP is provided via two connectors.

### 4.1 Connector J1

Connector J1 is a serial interface at 1.8V voltage level. A 14 pin 1.27mm pitch through hole connector is used. The pinout is shown in Table 1.

Pin 8 (GPIO[4]) is a pin that can be used to monitor NB1043AP status. It blinks for 1ms every time that some traffic is generated on the UART interface. It can be left unconnected if desired.

This interface port allows the user to download the firmware by using the interface board IB2000. Details on flash programming are available in the IB2000 datasheet.

**Table 1. Interface connector J1**

Pin #	Description
1	NVDD (3.3V)
2	NMEA TX
3	NMEA RX
4	GND
5	Reset
6	VBAT
7	DSU_MUX
8	GPIO[4]
9	DSU_RX
10	DSU_TX
11	DSU_EN
12	DSU_BRE
13	DSU_ACT
14	WAKEUP

### 4.2 Connector J2

On connector J2 the NJ1030A 8 GPIO signals are available at 1.8V voltage level. The analog input signal to A/D Converter AIN[2] is also available. A 12 pin 1.27mm pitch through hole connector is used. The pinout is shown in Table 2.

**Table 2. Interface connector J2**

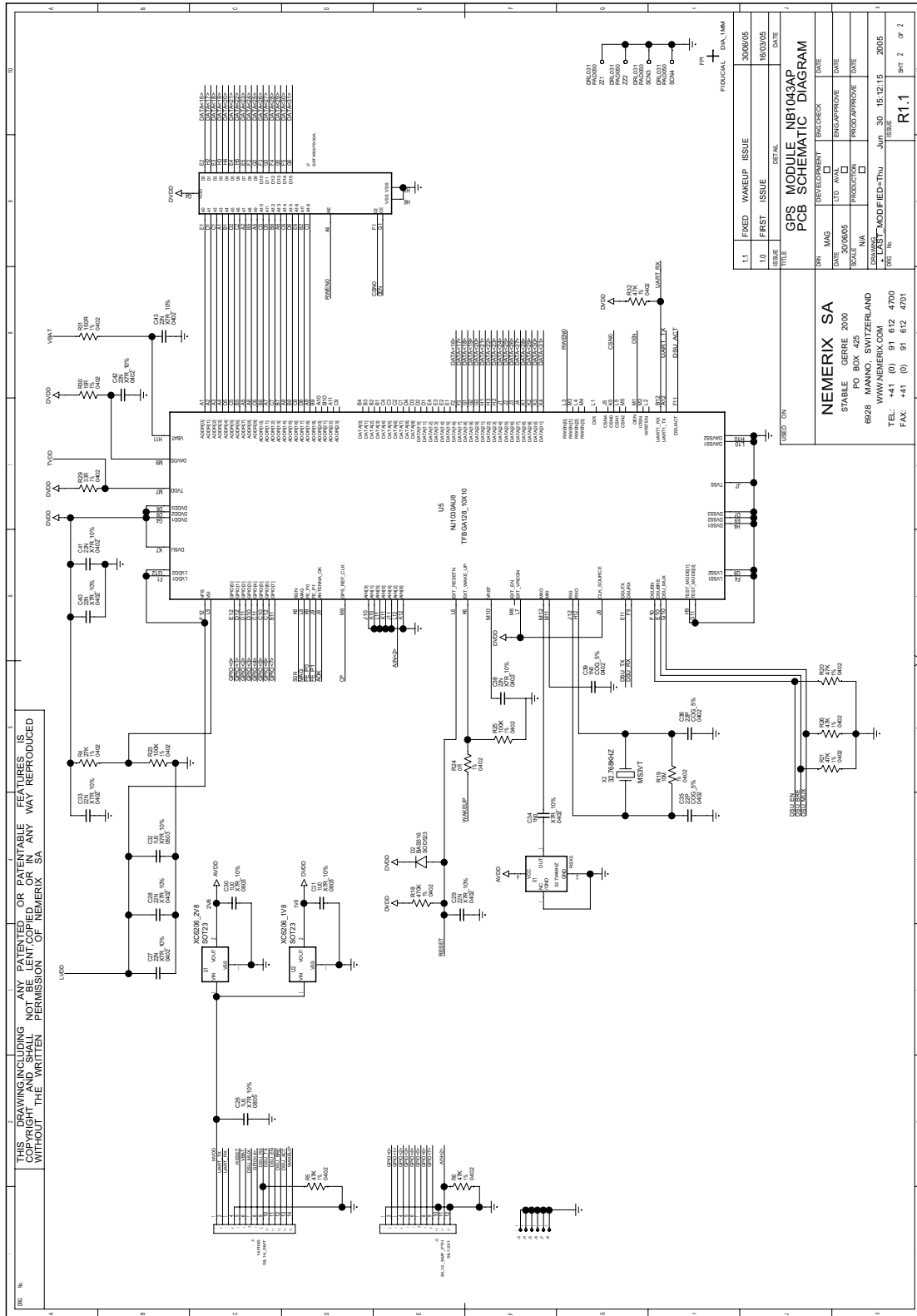
Pin #	Description
1	GND
2	GPIO[0]
3	GPIO[1]
4	GPIO[2]
5	GPIO[3]
6	GPIO[4]
7	GPIO[5]
8	GPIO[6]
9	GPIO[7]
10	GND
11	AIN[2]
12	GND

The NB1043AP is also SMT compliant and can be mounted directly on the host PCB without the need of the connectors J1 and J2.



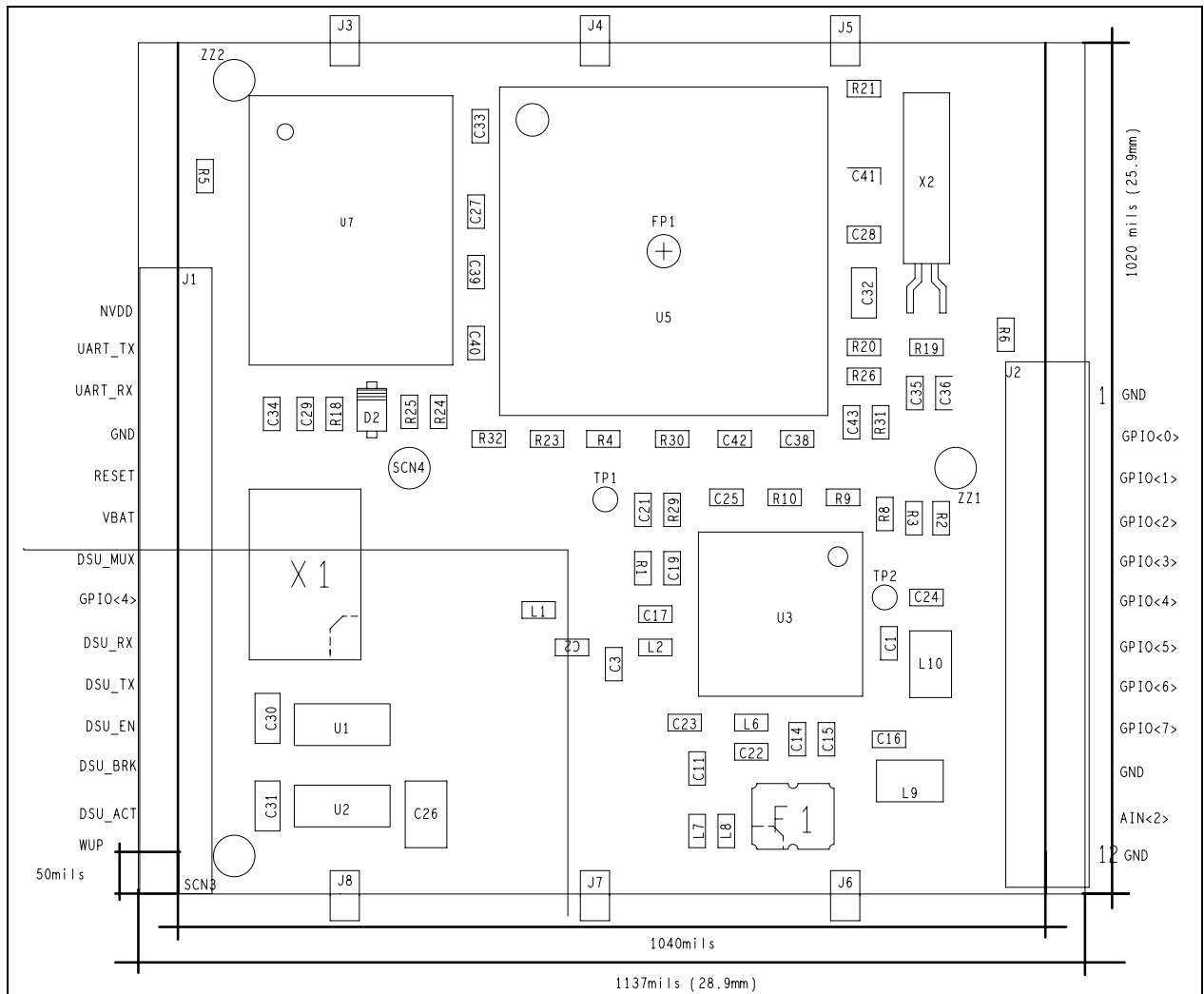
Schematic Diagram (Continued)

Figure 3. Base band section schematic diagram



## 6. PCB Layout

Figure 4. PCB top assembly





## 9 Bill of Material

Symbol	Type	Value	Size	Description
F1	Toyocom	TQS-949FA	2x2.5mm	GPS L1 SAW filter
J1	14x1 connector		1.27 mm pitch	Power supply and interface connector
J2	12x1 connector		1.27 mm pitch	Interface connector
A1	Patch antenna		25x25mm	L1 passive patch antenna.
C1 <sup>3</sup>	COG	33pF	0402	IF filter second tank capacitor
C2	COG	100pF	0402	LNA input DC block capacitor
C3	COG	0.56pF	0402	LNA input matching capacitor
C11	COG	100pF	0402	LNA output DC block capacitor
C14	COG	10pF	0402	NJ1006A Mixer input DC block
C15	X7R	100nF	0402	NJ1006A Band Gap reference decoupling
C16 <sup>3</sup>	COG	33pF	0402	IF filter first tank capacitor
C17	COG	470pF	0402	NJ1006A PLL loop filter capacitor
C19	X7R	100nF	0402	NJ1006A VB reference decoupling
C21	X7R	3.3nF	0402	NJ1006A PLL loop filter capacitor
C22	X7R	1nF	0402	NJ1006A AVDD decoupling capacitor
C23	X7R	22nF	0402	NJ1006A AVDD decoupling capacitor
C24	X7R	10nF	0402	NJ1006A AGC capacitor
C25	X7R	22nF	0402	NJ1006A TVDD decoupling capacitor
C26	X7R	1uF	0805	Main NVDD decoupling capacitor
C27	X7R	22nF	0402	NJ1030A LVDD decoupling capacitor
C28	X7R	22nF	0402	NJ1030A LVDD decoupling capacitor
C29	X7R	22nF	0402	NJ1030A reset capacitor
C30	X7R	1uF	0603	Main AVDD decoupling capacitor
C31	X7R	1uF	0603	Main DVDD decoupling capacitor
C32	X7R	1uF	0603	NJ1030A LVDD decoupling capacitor
C33	X7R	22nF	0402	NJ1030A DVDD decoupling capacitor
C34	X7R	1nF	0402	TCXO coupling capacitor
C35	COG	22pF	0402	RTC XTAL load capacitor
C36	COG	22pF	0402	RTC XTAL load capacitor
C38	X7R	22nF	0402	NJ1030A band gap reference decoupling
C39	X7R	1nF	0402	NJ1030A MXI decoupling
C40	X7R	22nF	0402	NJ1030A DVDD decoupling capacitor
C41	X7R	22nF	0402	NJ1030A DVDD decoupling capacitor
C42	X7R	22nF	0402	NJ1030A DAVDD decoupling capacitor
C43	X7R	22nF	0402	NJ1030A VBAT decoupling capacitor
D2	BAS516		SOD-523	Reset circuit diode
L1 <sup>1</sup>	Multi-layer	33nH $\pm$ 10%	0402	LNA ESD protection inductor
L2 <sup>1</sup>	Multi-layer	5.6nH $\pm$ 0.3nH	0402	LNA input matching inductor
L6 <sup>1</sup>	Multi-layer	33nH $\pm$ 10%	0402	LNA output bias inductor
L7 <sup>1</sup>	Multi-layer	2.2nH $\pm$ 0.3nH	0402	LNA output matching inductor
L8 <sup>1</sup>	Multi-layer	3.3nH $\pm$ 0.3nH	0402	LNA output matching inductor
L9 <sup>2</sup>	Multi-layer	1.5uH $\pm$ 10%	0805	IF filter first tank inductor
L10 <sup>2</sup>	Multi-layer	1.5uH $\pm$ 10%	0805	IF filter second tank inductor
R1	Chip	6.8k $\pm$ 1%	0402	PLL loop filter resistor
R2	Chip	390R $\pm$ 1%	0402	NJ1006A P1 output damping resistor
R3	Chip	390R $\pm$ 1%	0402	NJ1006A P0 output damping resistor
R4	Chip	27k $\pm$ 1%	0402	NJ1030A voltage supervisor resistor

R5	Chip	47k $\pm$ 1%	0402	NJ1030A DSURX pull-down resistor
R6	Chip	47k $\pm$ 1%	0402	NJ1030A AIN[2] pull-down resistor
R8	Chip	390R $\pm$ 1%	0402	NJ1006A SGN output damping resistor
R9	Chip	390R $\pm$ 1%	0402	NJ1006A MAG output damping resistor
R10	Chip	390R $\pm$ 1%	0402	NJ1006A CP input damping resistor
R18	Chip	470k $\pm$ 1%	0402	Reset circuit resistor
R19	Chip	10M $\pm$ 1%	0402	RTC oscillator bias resistor
R20	Chip	47k $\pm$ 1%	0402	NJ1030A DSU_EN pull-down resistor
R21	Chip	47k $\pm$ 1%	0402	NJ1030A DSU_BRE pull-down resistor
R23	Chip	100k $\pm$ 1%	0402	NJ1030A voltage supervisor resistor
R24	Chip	0R	0402	NJ1030A WAKEUP resistor
R25	Chip	100k $\pm$ 1%	0402	NJ1030A WAKEUP pull-down resistor
R26	Chip	47k $\pm$ 1%	0402	NJ1030A DSU_MUX pull-down resistor
R29	Chip	33R $\pm$ 1%	0402	NJ1030A TVDD filter resistor
R30	Chip	10R $\pm$ 1%	0402	NJ1030A DAVDD filter resistor
R30	Chip	150R $\pm$ 1%	0402	NJ1030A VBAT filter resistor
U1	Torex XC6206	2.8V	SOT-23	AVDD voltage regulator
U2	Torex XC6206	1.8V	SOT-23	DVDD voltage regulator
U3	Nemerix NJ1006AM5	LPCC28	5x5 mm	Nemerix GPS front-end
U5	Nemerix NJ1030AU8	TFBGA128	10x10 mm	Nemerix GPS base-band processor
U7	SST39WF400AM1	TFBGA48	6x8 mm	4Mbit flash memory.
(U7)	(SST39WF800AM1)	(TFBGA48)	(6x8mm)	(8Mbit flash memory)
X1	Rakon IT5325BE		4PADS5032	32.734MHz 2ppm TCXO.
X2	MC MS3V-T1R		XTAL_watch	32.768kHz Crystal for RTC.

**Note 1:** Avoid using wire wound inductors; MuRata LQG15H series works well.

**Note 2:** Use only multilayer fully shielded inductors, e.g. MuRata LQG21N1R5K10. 5% tolerance is recommended.

**Note 3:** 2% tolerance is preferred, 5% is acceptable.

## 10. Notes

### Ordering information

Part	Description
NB1043AP	GPS Engine Board

### Related documentation

Part	Description
IB2000_ds10	IB2000 datasheet
NJ1006A_ds13	NJ1006A datasheet
NJ1030A_ds13	NJ1030A datasheet

### Related products

Part	Description
IB2000	NB104xAx interface board
NJ1030AU5	GPS Baseband Processor BGA 7x7, 0.5mm pitch
NJ1030AU8	GPS Baseband Processor BGA 10x10, 0.8mm pitch
NJ1006A	GPS RF Front-End
EB1006AH11	NJ1006A GPS RF Front-End Evaluation board
DK1030A	Software Development Kit
NB1043AS	GPS Receiver Reference Design – active antenna

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