

1 General Description

The NB1846A is a reference design that can be used as an example to develop a self-contained GPS receiver module based on the Nemerix NJ1836A single package GPS receiver. The 8 MBit flash memory stores the Nemerix NS1030 GPS firmware.

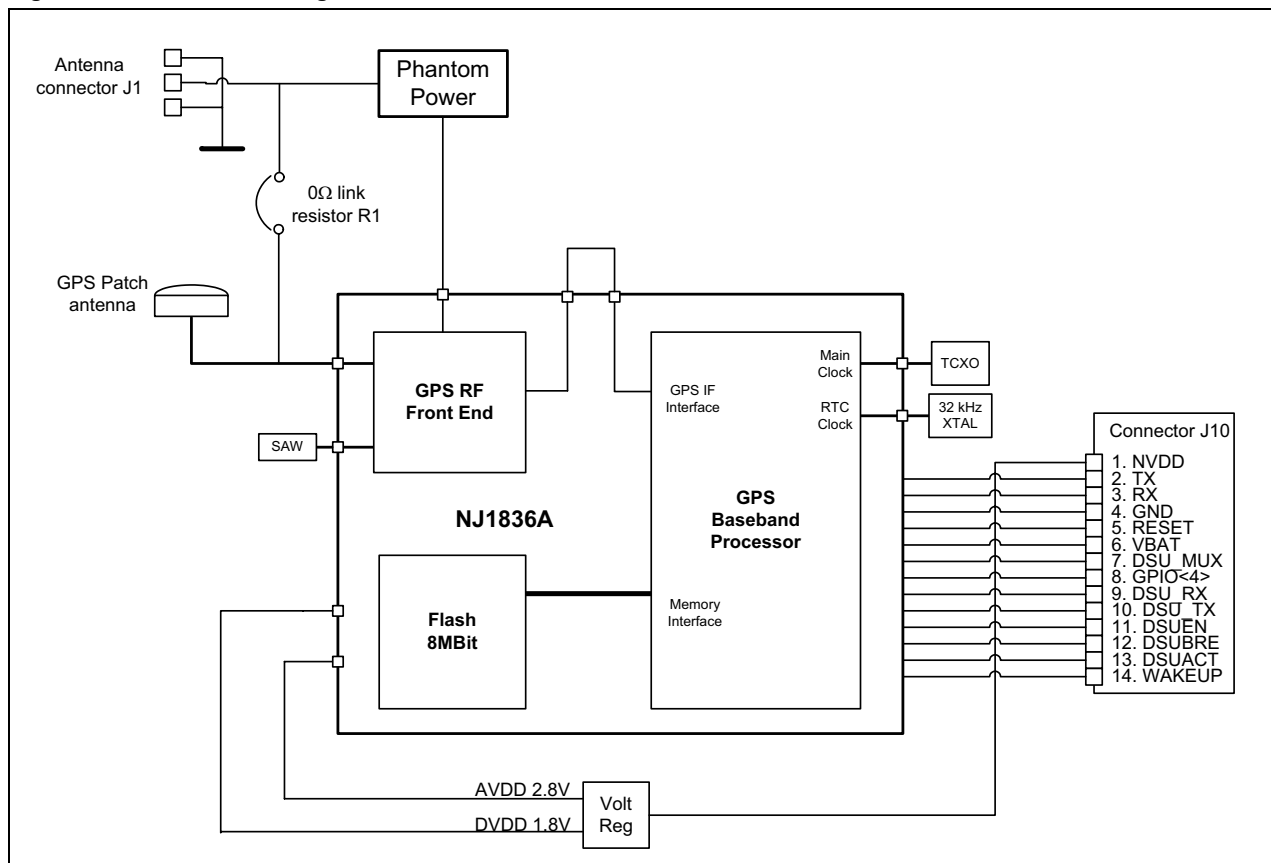
The NB1846A interfaces to the host system via the NJ1836A UART using the NMEA protocol expanded with Nemerix specific commands. It requires a 3.3V main power supply and a back-up voltage of 1.2V to 2V to implement maintain relevant GPS and system information in the non volatile portion of the NJ1836A memory.

The NB1846A is delivered with a 32.734MHz TCXO.

1.1 Features

- GPS receiver module supporting active or passive antenna
- Based on NJ1836A Single Package GPS Receiver
- Low power consumption: 19mA fully active
- Compact design: 21x16.4mm
- Support of WAAS/EGNOS (SW option)
- Supports 16.367MHz and 32.734MHz TCXO
- SMT compliant
- UART interface
- μ BGA 0.5mm pitch components

Figure 1. NB1846A Block diagram



1.2 Specifications

Parameter	Min	Typical	Max
Supply Voltage on (NVDD) pin	3V	3.3V	6V
Back up power supply voltage (VBAT)	1.2V		2V
Operating Temperature	-30°C		+65°C
Power Consumption in acquisition (fully active)		21mA	
Power Consumption in tracking (fully active)		17mA	
GPS Channels		16	
Tracking sensitivity	-150dBm		
TTFF Cold Start @ -135 dBm		46 sec	
TTFF Warm Start @ -141 dBm		34 sec	
TTFF Hot Start @ -141 dBm		5 sec	
Re-acquisition time @ -147 dBm		< 3 sec	
Update rate		1 Hz	

Frequency	1575.42MHz - L1 C/A Code
I/O Port	UART interface
Protocol	NMEA (Extended)
Weight	1.5g
Mating Connector	14 pin 1.27mm pitch headers
Dimensions	21x16.4x3.5mm (with shield)

2 Communication Protocol

The communication protocol is the standard NMEA expanded with NemerIX commands.

3 NB1846A Receiver Parts

3.1 Antenna

An active or passive antenna must be connected on the middle pin of connector J1. A phantom power (2.8V) is provided for the LNA of the active antenna. The current drawn by the antenna can be in the range of 2-20mA which is set by resistor R3. Outside of this current range the antenna detector on the NJ1836A RF front end will report an antenna issue (for more details see the NJ1836A datasheet).

A 12x12mm patch antenna can also be mounted on top of the NB1846A shield. In this case the resistor R1 and the connector J1 shall not be mounted.

3.2 NJ1836A Single Package GPS Receiver

The NJ1836A is used in its minimal configuration i.e. only as a GPS processor allowing the user to have an NMEA output from the module.

The power supply for the NJ1836A RF front end (AVDD) is set to 2.8V with a low dropout regulator. A single stage cascode integrated LNA with 20dB gain and 1.5dB NF has been used for best sensitivity. The LNA is noise matched allowing the use of a passive antenna or an external active antenna.

The NS1030 GPS firmware is stored into the NJ1836A integrated flash memory.

Power supply for the digital section is set to 1.8V (DVDD) with a low dropout regulator. Supply voltage for the core is set to 1.2V using the on-chip regulator. Communication to the NJ1836A is provided via the UART.

3.3 Clock

The clock frequency is set to 32.734MHz and is generated by a TCXO. The chosen TCXO is the Rakon IT5325B. It has 2.0ppm accuracy over temperature, a size of 5x3.2x1.5mm and requires a minimum voltage supply of 2.7V. The TCXO is sensitive to power supply noise, therefore the AVDD power supply of the RF front-end is used. The use of a 16.367 MHz TCXO is also possible in the design, if the WAAS/EGNOS functionality is not enabled in the GPS software.

RTC and Battery Backup

The NJ1836A includes a real time clock and 8kB NVRAM. This allows time and navigation database to be maintained on the NJ1836A when the NVDD power supply is powered down. The RTC crystal is a tuning fork type, 32.768kHz crystal. A Microcrystal CC5V-T1A in 4.1x1.5mm package is the selected device.

RTC and NVRAM require a supply voltage of 1.2V to 2V. Power must be provided via the VBAT pin on the interface connector. Any 1.2-1.5V battery or a super-capacitor can be used. If a rechargeable battery or a super-capacitor are used, a charge circuit must be provided. This may consist of a simple resistor-diode circuit. A mean to limit charge voltage below 2V should be included if the battery can be removed while the main power is on.

A suitable battery is the Varta V15H NiMH 1.2V rechargeable battery. This battery has a capacity of 15mAh and a size of 11.5mm(diameter)x3mm(height). It can be recharged at 1.8mA via a simple diode-resistor network. If the VBAT back-up voltage is not present RTC and NVRAM will not be active. As a consequence the receiver will always execute a cold start when activated.

3.4 Voltage Regulator

A dual voltage regulator generates two voltage supply (AVDD and DVDD) from the main voltage supply (NVDD). AVDD is 2.8V and provides voltage to the NJ1836A RF front end and the TCXO. DVDD is 1.8V and provides voltage to the NJ1836A GPS baseband processor and the internal flash memory. Power for the GPS baseband processor core is obtained with the internal voltage regulator and it is set to 1.2V.

The main voltage supply (NVDD) is continuously monitored using the analog to digital converted input AIN[2] of the NJ1836A. The A/D converter will saturate when the voltage on DVDD reaches 6.8V.

4 Interface Ports

4.1 Connector J10

Connector J10 is a serial interface at 1.8V voltage level. A 14 pin 1.27mm pitch SMT type connector is used. The pinout is shown in Table 1.

Pin 8 (GPIO[4]) is a pin that can be used to monitor NB1846A status. It blinks for 1ms every time that some traffic is generated on the UART interface. It can be left unconnected if desired.

This interface port allows the user to download the firmware in the flash by using the interface board IB2000. Details on flash programming are available in the IB2000 datasheet.

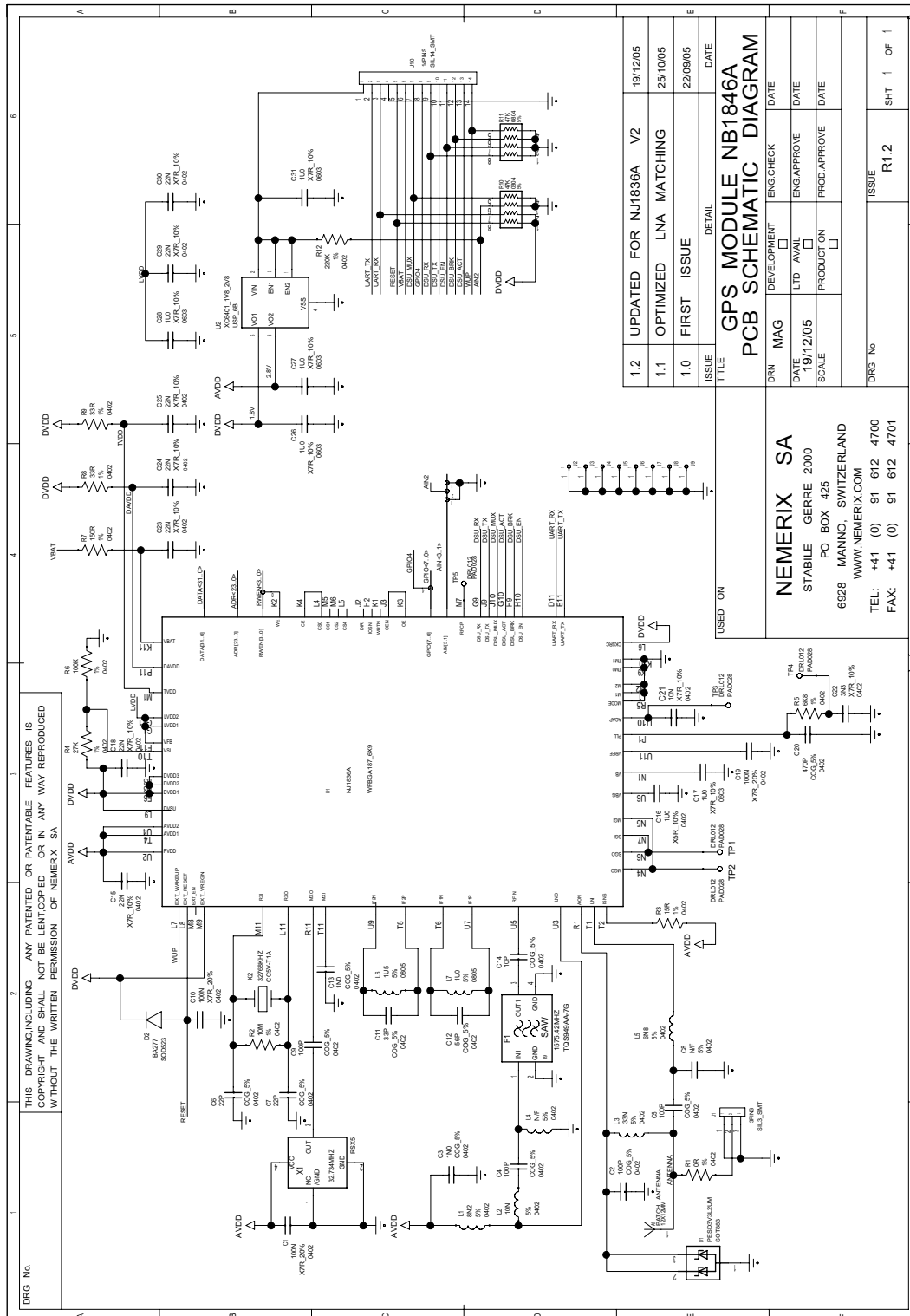
For interfacing the board with the IB2000, the NB1846A shall be soldered on the NB1846A socket board. The NB1846A socket board provides mechanical compatibility between the NB1846A and the IB2000.

Table 1. Interface connector J10

Pin #	Description
1	NVDD (3.3V)
2	NMEA TX
3	NMEA RX
4	GND
5	Reset
6	VBAT
7	DSU_MUX
8	GPIO[4]
9	DSU_RX
10	DSU_TX
11	DSU_EN
12	DSU_BRE
13	DSU_ACT
14	WAKEUP

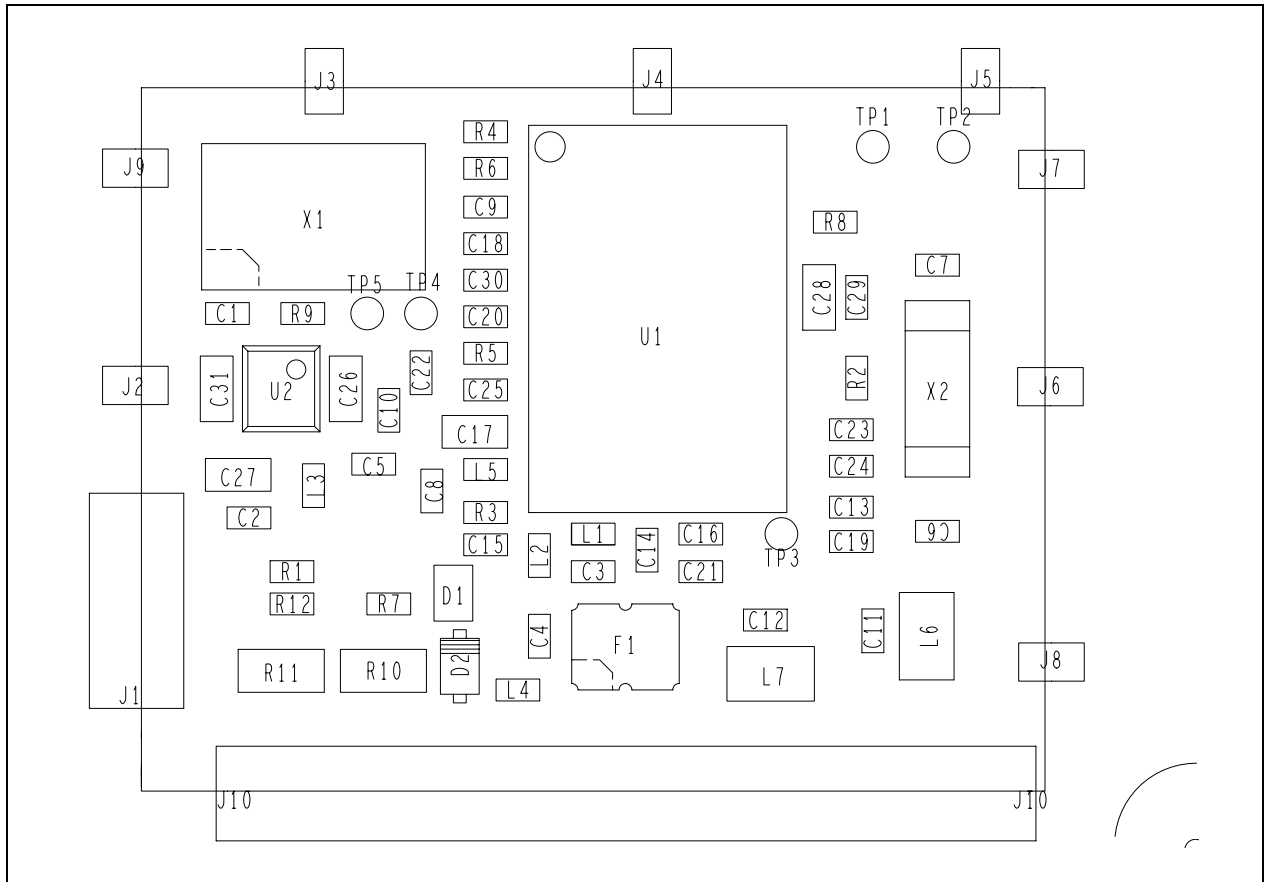
5. Schematic Diagram

Figure 2. NB1045A schematic diagram



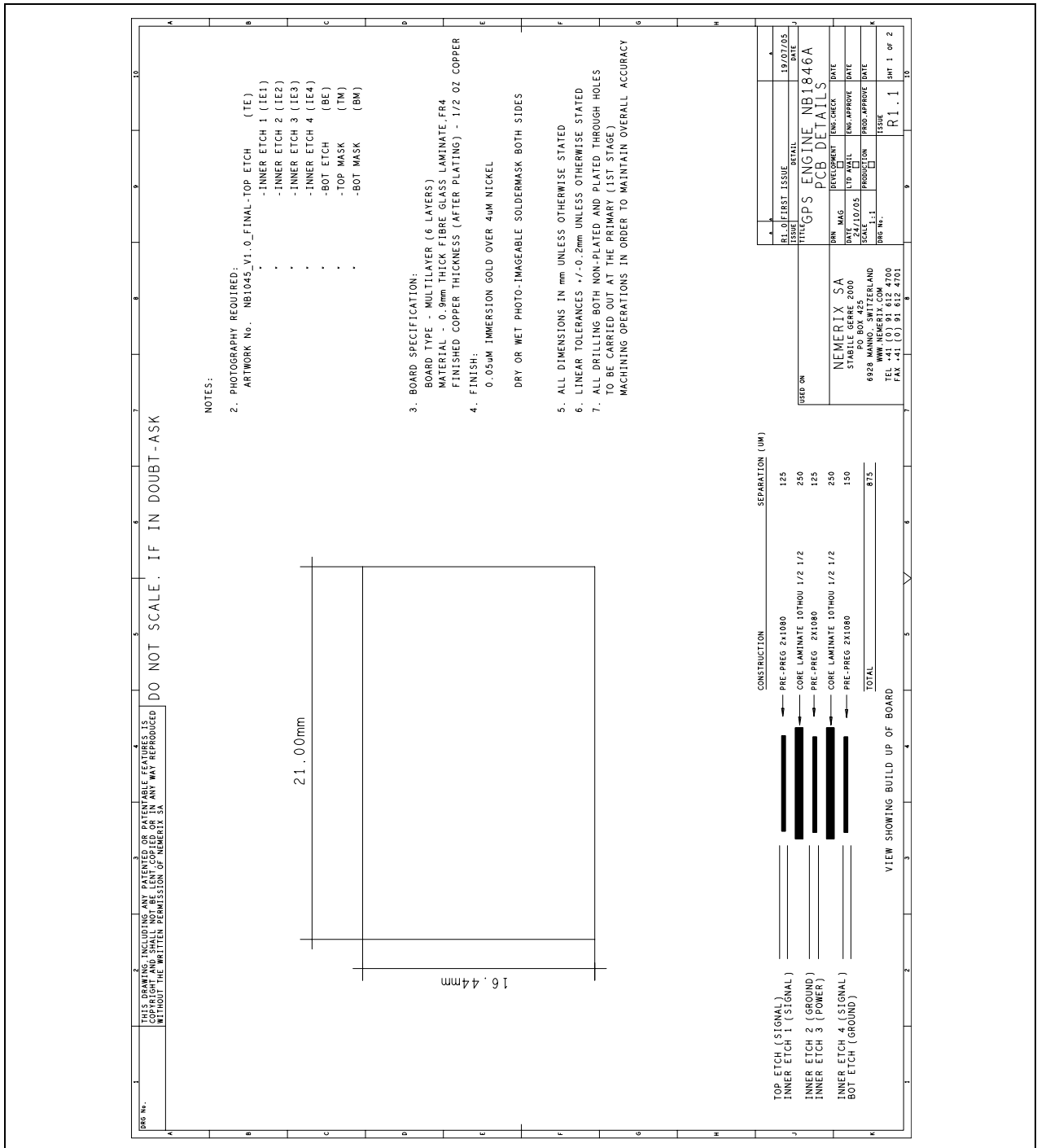
6. PCB Layout

Figure 3. PCB top assembly



7. PCB stack-up and details

Figure 4. PCB stack up and details



8. Physical drawings

Figure 5. Recommended PCB footprint

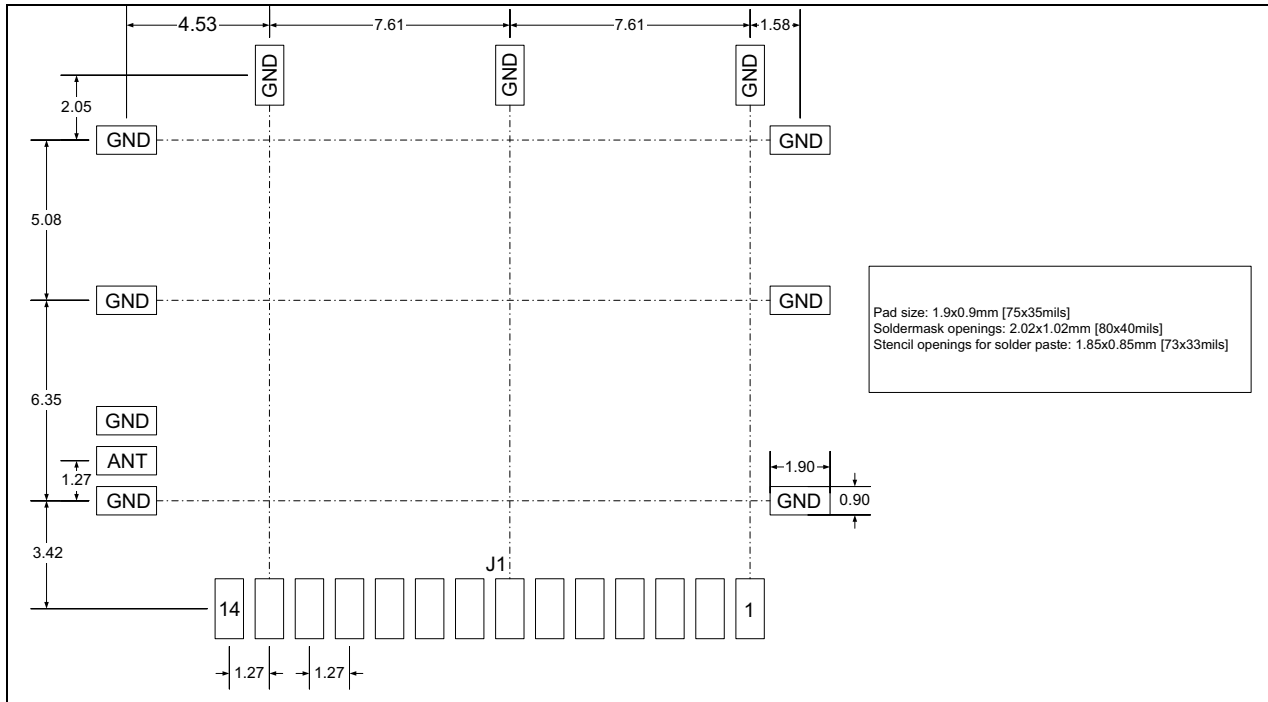
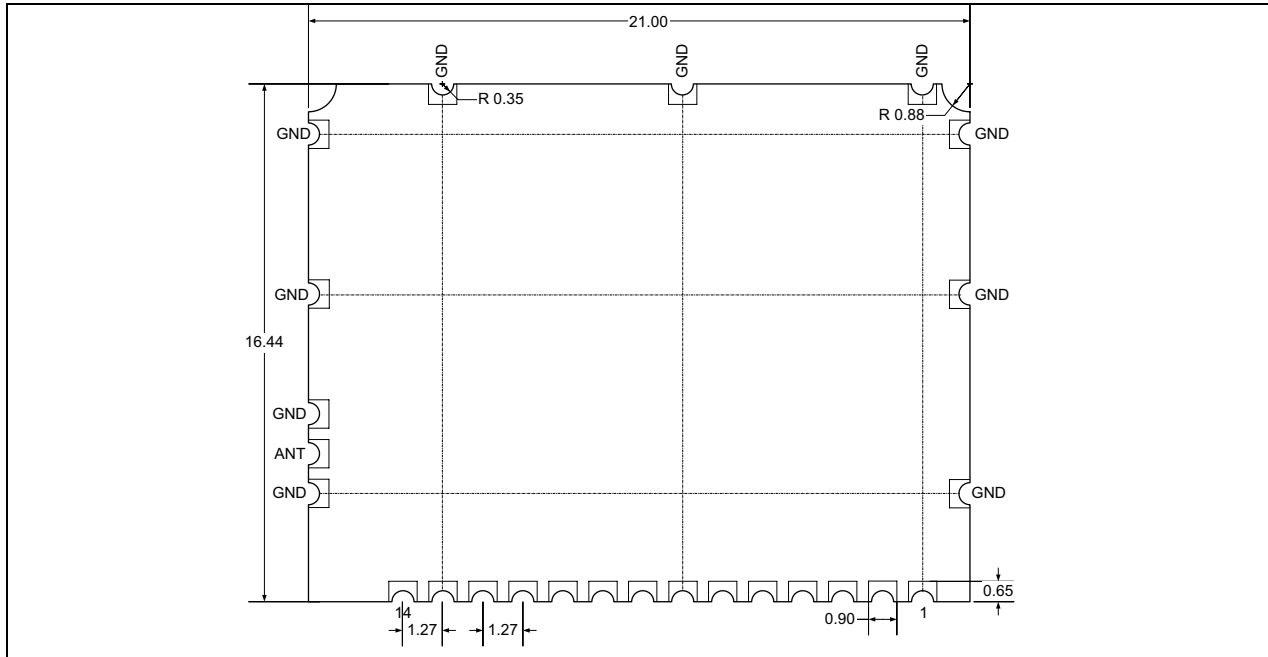


Figure 6. Physical dimensions



9 Bill of Material

Symbol	Type	Value	Size	Description
C1	X7R	100nF	0402	TCXO decoupling capacitor
C2	COG	100pF	0402	Antenna phantom power supply decoupling
C3	COG	1nF	0402	RF front end AVDD decoupling capacitor
C4	COG	100pF	0402	LNA output DC block capacitor
C5	COG	100pF	0402	LNA input DC block
C6	COG	22pF	0402	RTC crystal load capacitor
C7	COG	22pF	0402	RTC crystal load capacitor
C8		Not mounted	0402	LNA input matching capacitor
C9	COG	100pF	0402	TCXO coupling capacitor
C10	X7R	100nF	0402	Reset circuit capacitor
C11	COG	33pF	0402	2 nd IF filter tank capacitor
C12	COG	56pF	0402	1 st IF filter tank capacitor
C13	COG	1nF	0402	MXI decoupling capacitor
C14	COG	10pF	0402	Mixer input DC block capacitor
C15	X7R	22nF	0402	RF front end AVDD decoupling capacitor
C16	X5R	1uF	0402	RF front end VBG decoupling capacitor
C17	X5R	1uF	0603	RF front end VB decoupling capacitor
C18	X7R	22nF	0402	DVDD decoupling capacitor
C19	X7R	100nF	0402	Baseband processor VREF decoupling capacitor
C20	COG	470pF	0402	RF front end PLL loop filter capacitor
C21	X7R	10nF	0402	RF front end AGC capacitor
C22	X7R	3.3nF	0402	RF front end PLL loop filter capacitor
C23	X7R	22nF	0402	VBAT decoupling capacitor
C24	X7R	22nF	0402	DAVDD decoupling capacitor
C25	X7R	22nF	0402	TVDD decoupling capacitor
C26	X7R	1uF	0603	Main DVDD decoupling capacitor
C27	X7R	1uF	0603	Main AVDD decoupling capacitor
C28	X7R	1uF	0603	Main LVDD decoupling capacitor
C29	X7R	22nF	0402	LVDD decoupling capacitor
C30	X7R	22nF	0402	LVDD decoupling capacitor
C31	X7R	1uF	0603	Main NVDD decoupling capacitor
D1	PESD3V3L2UM		SOT-883	Antenna input ESD protection diode
D2	BA277		SOD-523	Reset circuit clamping diode
F1	Toyocom TQS949AA		2x2.5mm	GPS L1 SAW filter
L1	Multilayer	8.2nH	0402	LNA output matching inductance
L2	Multilayer	10nH	0402	LNA output matching inductance
L3	Multilayer	33nH	0402	Antenna phantom power RF choke inductance
L4		Not mounted	0402	LNA output matching inductance
L5	Multilayer	6.8nH	0402	LNA input matching inductance
L6	Multilayer	1uH ± 10%	0805	1 st IF filter tank inductance
L7	Multilayer	1.5uH ± 10%	0805	2 nd IF filter tank inductance
R1	Chip	0R	0402	External antenna connector link resistor
R2	Chip	10M ± 1%	0402	RTC oscillator bias resistor
R3	Chip	15R ± 1%	0402	Antenna detector current sense resistor
R4	Chip	27k ± 1%	0402	Voltage supervisor resistor
R5	Chip	6.8k ± 1%	0402	RF front end PLL loop filter resistor

R6	Chip	100k ± 1%	0402	Voltage supervisor resistor
R7	Chip	150R ± 1%	0402	VBAT protection resistor
R8	Chip	33R ± 1%	0402	DAVDD filter resistor
R9	Chip	33R ± 1%	0402	TVDD filter resistor
R10	Resistor array	47k ± 5%	0804	Pull ups and down resistor array
R11	Resistor array	47k ± 5%	0804	Pull ups and down resistor array
R12	Chip	220k ± 1%	0402	Supply voltage monitor resistor
U1	Nemerix NJ1836A		6x9mm	Nemerix single package GPS receiver
U2	Torex XC6401	1.8V / 2.8V	USP-6B	Dual low dropout voltage regulator
X1	Rakon IT5325BE	32.734MHz	4PADS5032	32.734MHz 2ppm TCXO.
X2	MC CC-5VT1A	32.768kHz	4.1x1.5mm	32.768kHz RTC crystal

10. Notes

Notes:**Ordering information**

Part	Description
NB1846A	GPS Engine Board

Related documentation

Part	Description
IB2000_ds10	IB2000 datasheet
NJ1x36A_ds01	NJ1x36A datasheet
NJ1006A_ds16	NJ1006A datasheet
NJ1030A_ds13	NJ1030A datasheet

Related products

Part	Description
IB2000	NB104xAx interface board
NB1846A socket	Adapter board for IB2000
NJ1836A	Single package GPS receiver with 8 Mbits flash memory
DK1030A	Software Development Kit

Nemerix SA
 Headquarters
 Stabile Gerre 2000
 PO Box 425
 6928 Manno
 Switzerland

Phone +41 91 612 4700
 Fax +41 91 612 4701
 email sales@nemerix.com

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