



1 General Description

The Nemerix NJ1006A is a highly integrated, low noise RF front-end for Global Positioning Systems (GPS) receivers targeted toward cost-sensitive portable and automotive applications. By integrating a low noise amplifier (LNA) and the tank-circuit of the local oscillator, the NJ1006A reduces both the bill of materials and PCB area substantially, enabling very small form factor implementations.

The NJ1006A is a double super-heterodyne receiver for the GPS L1 band. It is functionally and pin-to-pin compatible with the NJ1006. Main advantages are the lower power consumption and the lower noise integrated LNA that removes the need of an external LNA for passive antennas.

The on-chip LNA allows either a passive or an active antenna to be connected to the NJ1006A. A flexible PLL and a crystal oscillator are also provided. A reference frequency of 16.367 MHz, as well as all frequencies commonly used in all cell-phones are supported. The crystal oscillator may also be used as buffer for low amplitude TCXOs or may be disabled completely if desired.

An antenna detector and switch is available as a support function for systems requiring an active antenna such as automotive applications. The antenna detector is able to detect an open or shorted active antenna. In the latter case it also provides current limiting to protect both the antenna and the receiver from any damage.

The NJ1006A operates from 2.2 to 3.6V over a temperature range of -40 to +85°C, consuming only 6.9mA when fully active.

Four low-latency power-down modes are provided to aid in implementing various power-saving schemes.

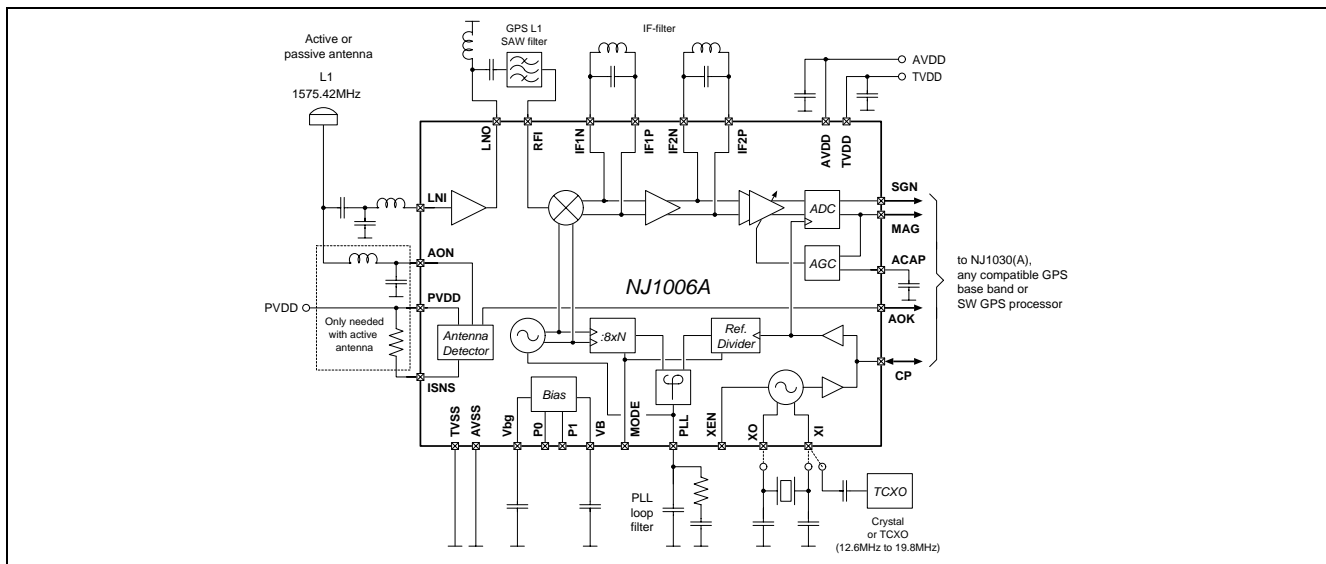
1.1 Features

- Highly integrated receiver for GPS L1 (C/A-code)
- Low BOM: 22 low cost components
- Low voltage operation – 2.2 to 3.6V
- Ultra low power consumption
 - Fully active – 6.9mA
 - Stand-by – 2.8mA
 - Doze – 450µA
 - Sleep – 10nA
- Accepts passive and active antennas
- Antenna detector with auto switch functionality
- Supports all cell-phone reference frequencies
- 2-bit digital output: sign and magnitude
- 28 leads 5x5 mm QFN package
- Lead-free, RoHS compliant package

1.2 Applications

- Battery operated GPS receivers
- Bluetooth™, remote GPS receivers
- Recreational/sport GPS receivers
- Software GPS receivers

Figure 1. Block Diagram



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2 Absolute Maximum Ratings

Max. Supply Voltage AVDD, TVDD	4V	Continuous Power Dissipation	300mW
Max. Supply Voltage PVDD	4V	Operating Temperature	-40 to +85°C
Max. RF Input	+10dBm	Junction Temperature	125°C
Max. current into any pin except ISNS and AON	±20mA	Storage temperature	-65 to +150°C
Max. current into ISNS and AON	+50mA	Lead temperature (Soldering, <40s).....	260°C
ESD Rating (HBM)	2kV		

Absolute maximum ratings are short term stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the recommended operating conditions is not implied. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.



ESD sensitive device: use proper precautions when handling this device.

3 Electrical Characteristics

AVDD=2.2V to 3.6V, TVDD = 1.6V to AVDD + 0.2V, PVDD=2.2V to 3.6V, T_{amb}=-40 to +85°C, no load, crystal oscillator active, unless otherwise noted. All voltages are referred to AVSS. Typical values are at AVDD = 2.5V, TVDD = 1.8V, PVDD=2.5V, T_{amb}=+27°C.

Parameter	Conditions	Min	Typ	Max	Unit	Notes
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LNA

Gain	power gain, noise matched		19		dB	1
Noise figure	noise matched		1.5		dB	1
1dB compression point	input referred		-25		dBm	1
IP3	input referred		-10		dBm	1
Input VSWR	noise matched		3:1			1
Output VSWR			1.1:1			1

RF Mixer

Conversion gain	voltage gain, no load	14	15	16	dB	2
SSB noise figure	differential output		9	11	dB	
1dB compression point	input referred		-18	-20	dBm	
Input VSWR	at 1.57GHz		1.1:1	1.4:1		
Diff. output resistance		950	1200	1450	Ω	3
Diff. output capacitance	parallel		1.5		pF	

IF Strip

1 st stage voltage gain	unloaded		15		dB	
Diff. output resistance		950	1200	1450	Ω	3
Diff. output capacitance	parallel		500		fF	
AGC amplifier gain			70		dB	
Gain control range		50	60		dB	
AGC sensitivity	pin 26	3.0	3.9	6.0	mV/dB	4,5
AGC volt. at max. gain	pin 26	0.77	0.90	1.05	V	4
AGC output current	peak, pin 26, at 25°C	13	20	29	μA	4,5
AGC hold leakage current	pin 26, at 85°C			10	nA	
ADC sensitivity	full scale (MAG=1)	75	100	115	mV	6
ADC SGN duty cycle			50		%	
ADC MAG duty cycle			33		%	

Electrical Characteristics - Continued

Parameter	Conditions	Min	Typ	Max	Unit	Notes
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Local Oscillator, PLL

VCO frequency range		1.35		1.8	GHz	
Phase noise	100kHz offset		-75		dBc/Hz	7
PLL spurs	recommended loop filter		<-60		dBc	
PFC gain	pin 11		7.96		$\mu\text{A}/\text{rad}$	
PFC output current	peak, pin 11		50		μA	
PFC voltage swing	pin 11	0.2		2.0	V	
PFC leakage current	pin 11, at 85°C			10	nA	

Crystal Oscillator

Crystal drive level			10		μW	8
Operating current			140		μA	
Clock duty cycle	pin4 , output	40	50	60	%	

Voltage Regulator

Bandgap ref. voltage	no load	1.12	1.18	1.24	V	
Bandgap ref. output current		200			μA	9
Bandgap load regulation	I(VBG)=0 to 200 μA		2	5	mV	
Regulator output voltage		1.80	1.91	2.0	V	
Regulator line regulation	AVDD 2.2V to 3.6V		4		mV	
Regulator output current		500			μA	9
Regulator load regulation	I(VB)=0 to 4mA		7	10	mV	

Digital Interface

Input high level		0.8 TVDD		TVDD+0.2	V	10
Input low level		-0.2		0.2 TVDD	V	10
Output high level	I _{OH} =-1mA	0.9 TVDD			V	11
Output low level	I _{OL} =1mA			0.1 TVDD	V	11
Output rise time	C _{load} =15pF			10	ns	12
Output fall time	C _{load} =15pF			10	ns	12

Antenna Detector and Switch

Low trip voltage			36		mV	
High trip voltage			300		mV	
Max. switch current	PVDD=2.2V	12			mA	
Max. switch current	PVDD=3.0V	24			mA	

Electrical Characteristics - Continued

Parameter	Conditions	Min	Typ	Max	Unit	Notes
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Power Supply

Supply voltage	analog	AVDD	2.2	2.5	3.6	V	
	digital	TVDD	1.6		AVDD+0.2V	V	
	antenna	PVDD	2.2		3.6	V	
Supply current	fully active	AVDD		6.4		mA	
		TVDD		500		µA	
	stand-by	AVDD		2.4		mA	
		TVDD		400		µA	
	doze, crystal osc. on	AVDD		300		µA	8
		TVDD		150		µA	8
	doze, crystal osc. off	AVDD		130	160	µA	
		TVDD		30		nA	
sleep	AVDD and TVDD		10	100	nA		

Note 1: LNA with recommended input and output matching networks (See section 11).

Note 2: Voltage conversion gain, differential, from RFIN to IF1 output, unloaded.

Note 3: I/O impedances track to 5% or better.

Note 4: Internal AGC regulator may be overridden by applying a control voltage to pin 26 (50µA minimum source capability recommended).

Note 5: This value is proportional to absolute temperature (PTAT).

Note 6: Voltage at ADC input (IF-amp output), which switches MAG output to 1.

Note 7: Closed PLL loop.

Note 8: Actual crystal drive level depends on crystal type and Q.

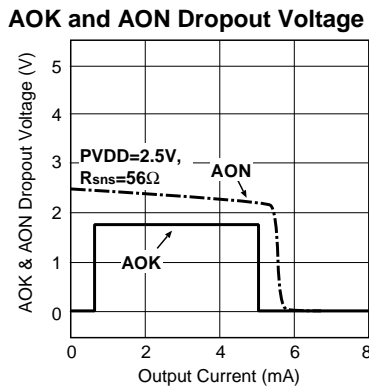
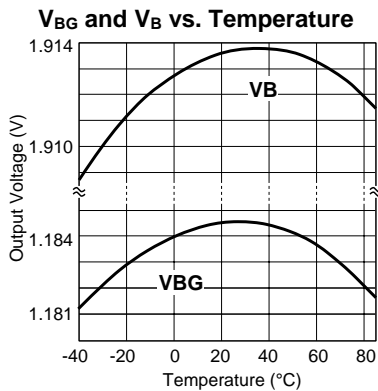
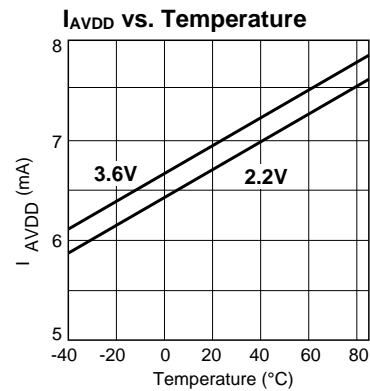
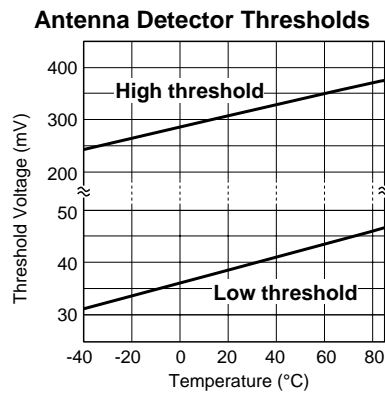
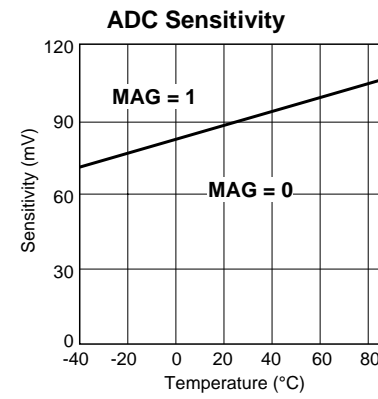
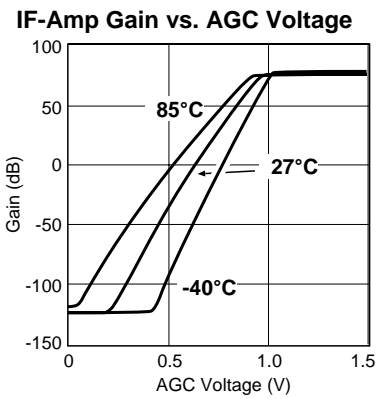
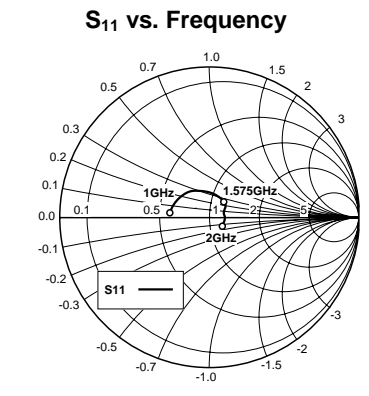
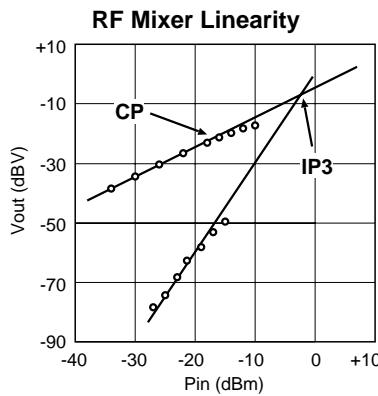
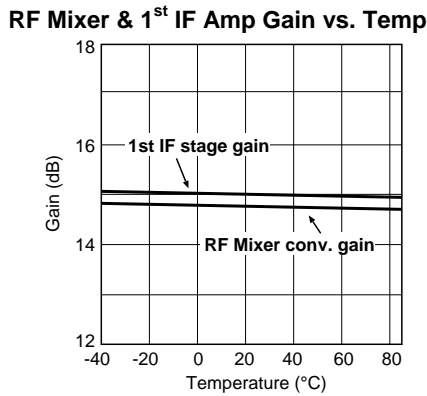
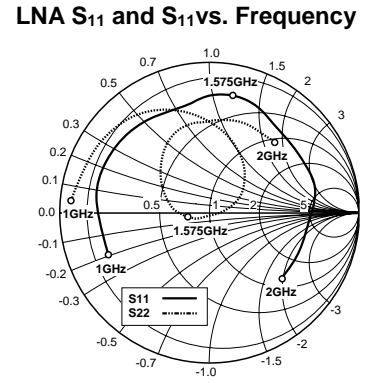
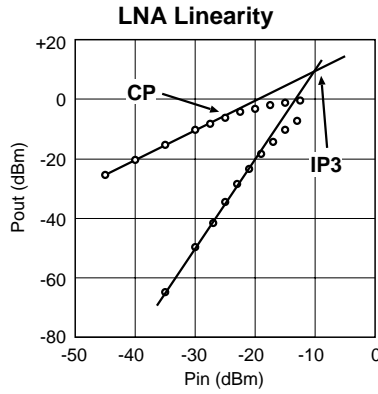
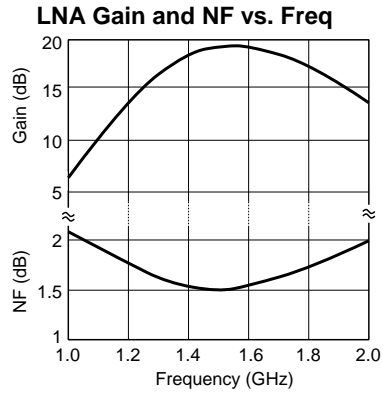
Note 9: Minimum current available to an external load under worst-case conditions.

Note 10: P0, P1 and CP only. The MODE pin should be tied either to AVSS or AVDD.

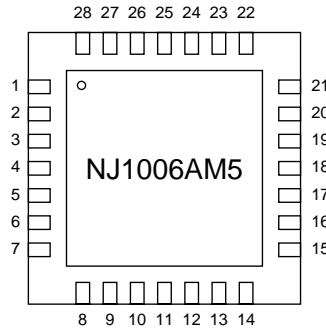
Note 11: SGN, MAG, CP and AOK.

Note 12: Measured between the 10% and 90% points. Load capacitance on these pins must be minimized (preferably below 5pF).

4 Typical Operating Characteristics



5 Pin Configuration



QFN 5x5mm Package (top view)

6 Pin Description

Name	QFN	Description
SGN	1	ADC sign bit data output. Synchronized to falling edge of CP.
MAG	2	ADC magnitude bit data output. Synchronized to falling edge of CP.
AOK	3	Antenna OK bit data output. Active high.
CP	4	Clock signal input/output.
TVSS	5	Digital negative power supply pin.
M2	(int. conn.)	Selects reference frequency operating mode.
TVDD	6	Digital positive power supply pin. Decouple to TVSS.
M1	(int. conn.)	Selects reference frequency operating mode.
XEN	7	Enable pin for the crystal oscillator. Enabled = 'high'.
AVSS	DAP	Analog negative power supply pin. Must be connected/soldered to PCB.
XO	8	Crystal oscillator output pin.
XI	9	Crystal oscillator input pin.
AVSS	DAP	Analog negative power supply pin. Must be connected/soldered to PCB.
VB	10	Output of the on-chip voltage regulator. Decouple to AVSS close to the chip.
PLL	11	Output of the PLL phase comparator. Connected to the loop filter.
AON	12	Power supply to active antenna.
AVSS	DAP	Analog negative power supply pin. Must be connected/soldered to PCB.
LNI	13	LNA input for the 1575.42MHz GPS L1 signal.
AVSS	DAP	Analog negative power supply pin. Must be connected/soldered to PCB.
ISNS	14	Sense current pin for the antenna detector.
PVDD	15	Antenna power supply pin.
LNO	16	LNA output.
AVDD	17	Analog positive power supply pin. Decouple to AVSS close to the chip.
AVDD	17	Analog positive power supply pin. Decouple to AVSS close to the chip.
AVSS	18	Analog negative power supply pin. Shield for RFIN.
RFIN	19	RF-mixer input signal. Impedance: 50Ω nominal.
VBG	20	1.2V bandgap reference output.
IF1P	21	IF-mixer output, 1 st stage IF-amp input. Connected to the external LC filter.
IF1N	22	IF-mixer output, 1 st stage IF-amp input. Connected to the external LC filter.
AVSS	DAP	Analog negative power supply pin. Must be connected/soldered to PCB.
IF2P	23	1 st stage IF-amp output, IF-AGC input. Connected to the external LC filter.
IF2N	24	1 st stage IF-amp output, IF-AGC input. Connected to the external LC filter.
MODE	25	Selects reference frequency operating mode.
ACAP	26	Connection to the AGC capacitor, sets the AGC time constant.
P1	27	Power control pin #1. Selects power down modes.
P0	28	Power control pin #2. Selects power down modes.

7 Equivalent Circuits

Pin	Description	Equivalent circuit
1 SGN 2 MAG 3 AOK (i.c.) M2 (i.c.) M1 5 MODE 7 XEN 27 P1 28 P0	Digital inputs and outputs. The <i>Mode</i> pin should be hard wired to either AVSS or AVDD. (The M1, M2 pins should be hard wired to TVSS or TVDD).	
4 CP	Clock input and output with pull down resistor. The <i>en</i> signal is derived from XEN.	
8 XI 9 XO	Crystal oscillator input and output (Pierce oscillator).	
11 PLL	PLL charge pump output.	
12 AON 14 ISNS 15 PVDD	Active antenna power switch and antenna detector circuitry.	

Equivalent Circuits (Continued)

Pin	Description	Equivalent circuit
13 LNI 16 LNO	LNA input and output.	
19 RFIN	RF Mixer input. Internally matched to 50Ω.	
21 IF1P 22 IF1N 23 IF2P 24 IF2N	IF input/output. capacitance shown includes parasitic capacitance of the package.	
26 AGC	AGC control circuit, gain control input (dB linear).	

8 Circuit Description

The NJ1006A is a super-heterodyne receiver front-end for the GPS L1 band characterized by a high degree of versatility. A typical receiver consists of an antenna, the NJ1006A, RF and IF filters and a crystal.

The signal path of the NJ1006A begins with the integrated LNA, which amplifies the RF signal. The LNA is a single stage cascode device that provides 19dB gain and 1.5dB NF when noise matched at the input and impedance matched at the output. The signal is then fed to the RF mixer, which converts the RF signal to the 1st IF. The mixer is single-balanced, provides 15dB typical gain and a 50Ω input impedance, which matches most existing filters for GPS use. The mixer output is directly connected to the IF amplifier internally. Two 2nd order balanced LC filters may be added at the input of the first 2 IF amplifier stages to select the desired signal bandwidth.

The filtered signal is then amplified by an IF amplifier with AGC. The AGC control circuit incorporates a hold function, which keeps the voltage at the AGC capacitor – and thus the amplifier gain – constant during circuit power-off periods. Subsequently, an ADC convert the 1st IF signal to a 2-bit digital word while at the same time effecting down-conversion to the 2nd IF by sub-sampling the 1st IF signal. The ADC has a positive temperature coefficient and as such partly compensates the negative TC of the IF amplifier. The 2-bit digital word (sign and magnitude) is suitable for direct interface to a base-band processor.

Local oscillator signals are generated by an internal fixed-frequency PLL. The local oscillator is a fully integrated balanced VCO. Its output is divided with an ECL divider and supplied to a phase frequency comparator. This block includes a hold function to maintain the VCO control voltage at approximately the correct value during a power-down phase, for faster restart of the VCO and minimum lock time when active mode is restored.

The reference frequency is provided by an on-chip crystal oscillator. The generated clock signal corresponds to the sampling clock of the A/D converter. An on-chip regulator supplies 1.9V to the VCO and to the VB pin. By connecting the XEN pin to TVDD, the crystal oscillator is enabled and the reference clock signal is available on pin CP where it may be used to drive the base-band processor, the control-

ling microprocessor and other functional blocks where desired. A low logic level on XEN disables the crystal oscillator, and an externally generated reference clock may be applied to CP.

The NJ1006A includes an antenna detector and switch. The antenna detector controls power supplied to an active antenna, and is able to detect both opens and short-circuits. A current limiter limits the antenna current to a safe level in the case of a short-circuit, in order to protect both the NJ1006A and the antenna.

Two power control pins select one of the three low-latency operating modes, to aid in implementing various power-saving schemes under control of the CPU and a power-down mode in which the NJ1006A is completely off and only leakage currents exist.

The NJ1006A directly interfaces to the NJ1030(A) base-band processor. When used with the NJ1030(A) all frequency plans are available, while the power modes are driven directly in a transparent way. Other base-band processors may be used as well, as long as they support one of the frequency plans required by the NJ1006A.

9 Frequency Plans

The NJ1006A supports various reference frequencies, leading to different frequency plans. A first reference frequency, 16.367MHz, is directly compatible with many existing base-band processors and is therefore an ideal choice in applications where the NJ1006A substitutes a previous generation front-end circuit. Most of the reference frequencies used in cellular phone standards are also supported. This allows the NJ1006A to share the same TCXO and simplify integration of GPS functionality into the phone. Selection of the reference frequency is effected by bonding options during packaging and by the logic level at pin MODE. Four different packaged versions are available (see Ordering Information), and in each of them the MODE pin selects between two or three different frequency plans. The MODE pin should be hard-wired to either AVDD or 0 since the choice of reference frequency is a system issue which dictates different IF frequencies, external component values and possibly affects settings in the base-band processor or processor firmware. The NJ1006A frequency plans are shown in Table 1.

Table 1: Supported frequency plan

Device	MODE	Ref. frequency	1 st IF frequency	2 nd IF frequency	LO frequency	Image frequency
NJ1006AH	0	16.367MHz	20.55MHz	4.188MHz	1554.86MHz	1534.31MHz
	AVDD	13.000MHz (GSM)	16.58MHz	3.58MHz	1592MHz	1608.58MHz
NJ1006AI	0	19.800MHz (CDMA)	24.42MHz	4.62MHz	1599.84MHz	1624.26MHz
	AVDD	19.200MHz (CDMA)	23.25MHz	4.051MHz	1552.17MHz	1528.92MHz
	AVDD	19.680MHz (CDMA)	15.55MHz	4.127MHz	1590.97MHz	1606.52MHz
NJ1006AJ	0	14.400MHz (PDC)	18.18MHz	3.78MHz	1593.60MHz	1611.78MHz
	AVDD	12.600MHz (PDC)	21.87MHz	3.328MHz	1597.29MHz	1619.16MHz
NJ1006AK	0	16.367MHz	20.55MHz	4.188MHz	1554.86MHz	1534.31MHz
	AVDD	15.36MHz (WCDMA)	18.94MHz	3.58MHz	1556.48MHz	1537.54MHz

10 Power Control

The NJ1006A provides 4 different low latency power modes that can be used to implement various power saving methods:

- **Sleep:** in sleep mode all parts of the NJ1006A, including the crystal oscillator, are powered down. In this mode no clock signal is generated and current consumption consists mainly of leakage currents.
- **Doze:** in doze mode the crystal oscillator is turned on while the rest of the NJ1006A remains off. The reference voltage and the voltage regulator are also turned on. In this state the crystal oscillator is operating (if enabled) and the clock signal is available on pin CP. The time required to enter this state is dominated by the time required by the crystal oscillator to start, and increases if a good quality crystal is used.
- **Stand-by:** in stand-by mode the PLL is turned on while only the signal path stays powered down. This state may be used to allow the PLL to stabilize before entering the fully active mode.
- **Fully active:** in fully active mode the NJ1006A is fully on and operating. The antenna detector is turned on to enable an external active antenna.

The power modes of the NJ1006A may be selected with pins P1 and P0. These are CMOS compatible, level sensitive (unregistered) static inputs. Table 2 shows the coding of P1 and P0 together with the approximate time required to reach stable operation (latency) from the previous state. Exiting any power mode is much faster and typically takes less than 100µs. Gray coding has been used to simplify avoiding glitches while switching from one power mode to the other.

Switching from one power mode to the other may be done in any order. If the on-chip crystal is used however, it is particularly important to avoid glitches to the low state on both P1 and P0, as these will disturb the reference crystal oscillator by turning it off during the glitch. When switching from 'Doze' to 'Fully active', it is therefore recommended that 'Stand-by' is selected first.

Table 2: Power modes

Mode	P1	P0	Latency
Sleep	0	0	-
Doze	0	1	10ms (Xosc-off) 50-100ms (Xosc-on)
Stand-by	1	1	5-10ms (depends on PLL loop filter)
Fully active	1	0	150-250µs

If an external crystal oscillator is used, no restriction exists in selecting power modes. Selection may be done to minimize latency or power consumption as desired. In systems that use long (>100ms) on-off times, switching from 'Sleep' to 'Fully active' is likely the best way to save power. This

may be achieved by toggling P1, with P0 hard-wired to TVSS.

11 Low Noise Amplifier

The LNA RF input (LNI) receives the 1575.42MHz GPS L1 signal. Matching networks are required at the LNA input and output. Noise matching at the input for best noise performance and impedance matching to match the 50Ω SAW filter at the output are recommended when a passive antenna is used. Recommended configuration and components values are shown in Figure 2. These values may vary depending on the layout of the PCB and may require optimization.

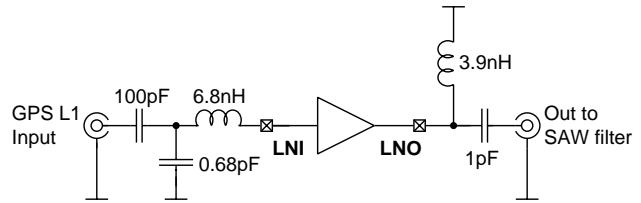


Figure 2: LNA input and output matching networks

In case a low gain (10-15dB) active antenna requiring impedance matching at the output is used, impedance matching the LNA input is recommended. If a high gain (25-30dB) antenna is used, it is recommended to turn-off the integrated LNA by connecting LNI pin to AVSS and letting LNO pin floating. In this case, the GPS signal will be directly fed to the RF mixer input (via a SAW filter if a suitable one is not included in the antenna).

12 Mixer RF Input

The mixer RF input pin (RFIN) receives the GPS signal amplified by the LNA. It is internally matched to 50Ω and is biased to about 400mV. Therefore it can be connected directly to most SAW filters without particular precautions.

This input should not be DC shorted to ground or receive any DC biasing from outside. In such cases a DC blocking series capacitor should be used. Such capacitor may also be used to compensate eventual stray inductance of the chip package and the PCB trace.

13 RF Filter

A filter is always required at the input of NJ1006A mixer, in order to remove out-of-band signals that could disturb chip performance. A filter with sufficient selectivity should be chosen. The two most important filter parameters are a sufficient attenuation of the image frequency (≥20dB recommended) and a sufficiently low insertion loss, especially if passive antennas and no external LNAs are used (≤2.5dB recommended). A SAW filter, such as MuRata SAFSE1G57AB0T10 works well. Dielectric filters are not recommended as they rarely have sufficient selectivity and are quite bulky.

14 IF Filter

The NJ1006A requires an external IF filter for channel selection and to filter noise at the images of the A/D con-

verter. This filter should be centered at the IF corresponding to the frequency plan chosen (see Table 1). The bandwidth of the IF filter should be adapted to the requirements of the base-band processor. In most cases a bandwidth of at least 2MHz is required, while a bandwidth larger than about 6MHz results in losses due to ADC image frequencies. A good trade-off between filter performance, size and cost, is the 4th order LC band-pass filter shown in Figure 3 for a 16.367MHz reference frequency. With the values shown, the filter is centered at 20.46MHz and has a bandwidth of about 4MHz to accommodate component tolerances of ±5%.

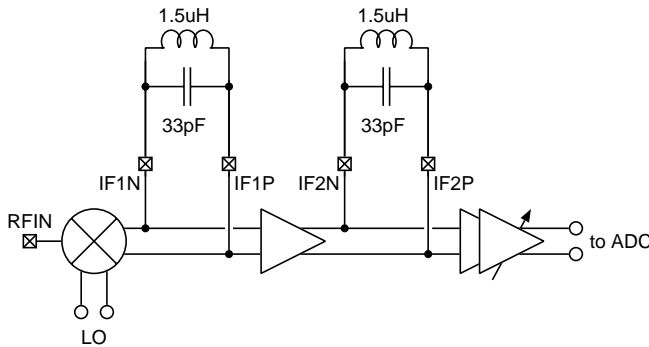


Figure 3: IF filter with components value (20.46MHz)

If a different frequency plan is chosen, the component values must be adapted accordingly. To avoid too high insertion losses, LC combinations with inductors values ≥1uH are recommended.

The inductors should be either air-core wire-wound or fully shielded ferrite core multi-layer type. The latter type is recommended especially when size is critical. Unshielded ferrite core inductors should be avoided since they will act as efficient ferrite antennas and will pick up interference (e.g. digital noise) too easily.

15 IF Amplifier

The IF amplifier has about 70dB of gain and 50dB of gain control range, which is sufficient to accommodate a wide range of input signals without saturation. A differential amplifier structure has been used to achieve rejection to common mode signals. This, together with usual shielding and layout practice, gives to the receiver very good robustness against interfering signals, possibly coming from the environment around the NJ1006A.

16 AD Converter and AGC

The IF signal is digitized by a 2-bit sign/magnitude AD converter. SGN and MAG represent the sign and the magnitude of the digitized IF signal. The 4 possible levels are coded as shown in Table 3.

The AGC uses the MAG signal as the regulation variable, and sets the gain of the IF amplifier to achieve state ‘high’ on the MAG output for about 33% of the time. The AGC regulator uses ratioed current sources, that source 10µA and sink 20µA from the ACAP pin. The time constant of the AGC is set with the capacitor connected to pin ACAP.

Table 3: Coded output signal

SGN	MAG	Value
0	1	+3
0	0	+1
1	0	-1
1	1	-3

The internal AGC regulator may be overridden by forcing a control voltage to pin ACAP. This will disable the internal AGC regulator. An external AGC loop may be useful if a different MAG duty cycle, faster response or infinite hold times are desired. To achieve full regulation under all possible conditions, this voltage should be supplied by a source having fairly low output impedance, and should be variable over the 0.1V to 1.1V range. A minimum source capability of 50µA is recommended. A typical op-amp or voltage mode DAC with a reference voltage of 1.2V are suitable sources. It is important that the voltage source doesn’t swing negative or above AVDD. A small capacitor – 1nF or so – may still be connected to the ACAP pin, to filter off possible noise from the control voltage.

The SGN output may be used as the IF output in systems using a 1 bit input. Its duty cycle is fixed to 50% and cannot be changed. An offset duty cycle on the SGN output is always due to interference between circuits operating at the clock frequency and the RF input or the IF filter of the NJ1006A (synchronous rectification).

17 Frequency Synthesizer

The NJ1006A contains a frequency synthesizer which generates the required local oscillator signal. Seven different division ratios are available to fit the eight supported frequency plans (Table 1), and are selected by choosing one of the four packaged version and via MODE pin.

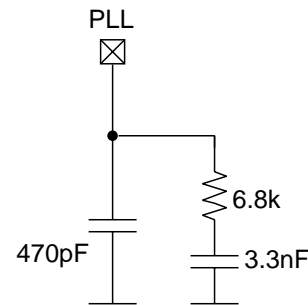


Figure 4: PLL loop filter

The loop filter of the PLL is external and is mounted directly close to the PLL pin. The 2nd order loop filter shown in Figure 4 realizes a classical 3rd order PLL with a bandwidth of 20kHz and a phase margin of 51 degrees. It has a relatively low spurious output which is sufficient in most applications. If a different PLL dynamic is desired, the loop filter may be redesigned accordingly. A faster PLL will result in lower phase noise close to the carrier at the expenses of higher spurious signals (centered at reference frequency).

multiples). A phase margin around 50-55° is recommended, as this results in fastest lock time.

The voltage swing on the on-chip tuning varactors can vary between 0.4V and 1.5V. This value can be directly measured on the PLL pin and in nominal conditions should be about in the middle of the tuning range (around 0.9V-1.1V).

18 Crystal oscillator

The reference clock signal may be either generated by the on-chip crystal oscillator, or supplied externally. Either a full swing CMOS compatible signal or a clipped sine are accepted by the NJ1006A.

The on-chip crystal oscillator is a Pierce oscillator. The external components required are the crystal resonator and its load capacitance. The schematic diagram of the resonator is shown in Figure 5.

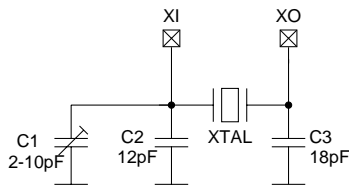


Figure 5: Crystal osc. resonator (assumes CL=10pF)

As in most oscillators, the performance is determined more by the resonator rather than the oscillator circuit, thus proper choice of the resonator is important. Here a high quality crystal for communication applications, such as NDK NX5032SA or NX4025GA is recommended. The load capacitors (C2 and C3 in Figure 5) must be approximately equal and should be set to twice the rated load capacitance (CL) specified by the crystal manufacturer. Good quality NPO ceramic capacitors are recommended for best oscillator stability. Stray capacitance (about 1.5-2pF) should also be taken into account. If desired a trimmer capacitor (C1) may be added in parallel to C2 for fine frequency adjustment.

The on-chip crystal oscillator is enabled by setting pin XEN to TVDD while it is disabled by setting pin XEN to TVSS. Pin XEN should never be left floating.

The XI pin can also be used as input for a typical TCXO signal. In this case, the oscillator must be enabled (XEN=TVDD) and will act as buffer for the TCXO signal. A full swing clock signal will be available on pin CP. The XO pin must be left floating. The circuit is shown in Figure 6.

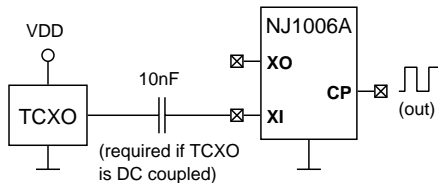


Figure 6: Connection to a TCXO.

19 Voltage Reference and Regulator

Biasing to the NJ1006A is provided by an on-chip 1.18V band-gap voltage reference and a 1.91V voltage regulator. These voltages are available on pins VBG and VB respectively. The 1.91V regulator provides power to the VCO and the crystal oscillator.

Both outputs may supply power to an external load if desired. The maximum load is 200µA and 500µA respectively. It is however important that these loads, if used, do not introduce any noise into VBG and VB. In particular, noise into VBG may disturb the IF-strip, while noise into VB may disturb the VCO and PLL. In a typical application VBG may be used as reference for a D/A converter for external AGC control.

VBG and VB are active in doze mode and up. They require at least 10nF (X7R) decoupling capacitors mounted close to the chip, although at least 100nF is recommended for VB. These capacitor values may be further increased, if desired.

20 Antenna Detector

An antenna detector and switch is integrated on the NJ1006A. It is intended to supply power and control an active antenna (if used). A typical configuration for a phantom powered antenna drawing 2-3mA is shown in Figure 7.

The antenna detector checks if the active antenna is properly connected to the receiver by checking the current consumed by the antenna. If the current is within specific margins the AOK pin is asserted, else it is set to low. An internal switch turns on the active antenna when the NJ1006A is set to active mode, while limiting the current to a safe value in case the antenna is shorted.

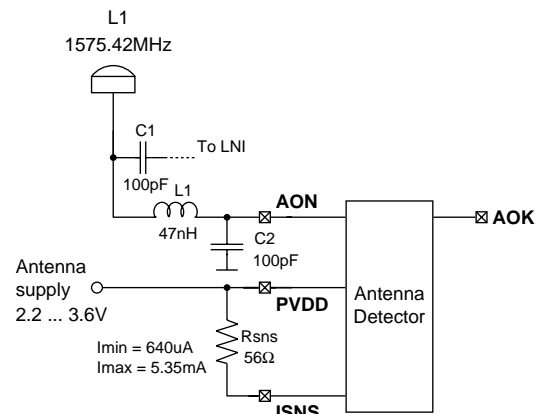


Figure 7: Antenna detector

The antenna power supply must be connected to pin PVDD. Voltages in the range between 2.2V and 3.6V are supported. The actual voltage supply for the antenna is available on pin AON.

External resistor Rsns between PVDD and ISNS is used to set the short and open current thresholds. The antenna detector measures the voltage drop (and thus the current) on resistor Rsns. Minimum and maximum voltage thre-

sholds are set to 36mV and 300mV, respectively. The corresponding minimum and maximum current is set by the external resistor R2 value:

$$I_{\min} = 36\text{mV}/R_{\text{sns}} (= 640\mu\text{A for a } 56\Omega \text{ resistor})$$

$$I_{\max} = 300\text{mV}/R_{\text{sns}} (= 5.35\text{mA for a } 56\Omega \text{ resistor})$$

If the voltage drop is between 36mV and 300mV the detector assumes the antenna is working properly and returns a high on the AOK pin. If the voltage drop is below 36mV AOK pin is set to low. In case a voltage drop higher than 300mV is measured, AOK is set to low and the output current is limited to around 10% above the maximum value. For best overall performance, I_{\max} should be set to about twice the typical current consumption of the active antenna. When the NJ1006A is in a power mode different than fully active, AOK is always low.

Antenna detector and switch may be used independently if desired. By connecting L1 and C2 to ISNS instead than AON, the antenna switch is bypassed, while by shorting PVDD to ISNS the antenna detector is bypassed (AOK will be always low). In these two cases the short-circuit protection is however lost and must be provided externally. If no active antenna is used, PVDD must be grounded, while AON and ISNS may be either grounded or left open. AOK will be always high when the NJ1006A is in active mode and always low when it is in any other power mode.

21 Digital I/O

The digital outputs SGN, MAG, CP and AOK are CMOS compatible and swing from 0V to TVDD. The SGN and MAG signals change on the falling edge of the CP and should be read in by the base-band processor on the rising edge of CP. The timing diagram is shown in Figure 8.

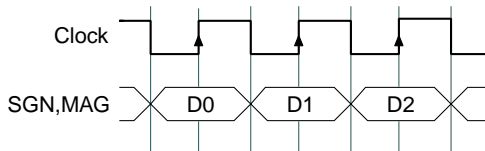


Figure 8: Digital output timing diagram

The CP pin can be used either as clock input or output. By enabling the on-chip reference crystal oscillator (XEN=TVDD), the CP pin becomes an output. It delivers a CMOS signal at the same frequency as the crystal oscillator, with a nominal duty cycle of 50%. By disabling the on-chip crystal oscillator, CP is turned to an input, which accepts an external clock signal with logic levels TVSS and TVDD and a duty cycle between 40% and 60%.

The AOK pin is active high and swings from TVSS to TVDD. This signal is latched and will change on the rising edge of the clock.

The digital outputs of the NJ1006A are quite weak, and capacitive loading to these pins should be minimized. An excessive load, in fact, will cause interference to the analog part of the chip due to switching noise. It is recommended that these outputs are loaded with a maximum of 2-4pF (i.e.

one typical digital output) and that PCB traces to these pins are kept short and routed away from the IF filter. If more drive is required, a buffer should be used, but attention must be paid to avoid interference between the buffer and the RF input or IF filter. Complete shielding may be required, especially if the antenna is mounted close to the receiver. Series damping resistors (220-470Ω), mounted close to the NJ1006A, are also recommended.

P1 and P0 are CMOS compatible inputs that should swing from TVSS to TVDD. These are level sensitive, unregistered inputs that operate whether the clock is present or not. It is therefore mandatory to avoid glitches on these signals. A glitch to low on both inputs in particular will disturb operation of the crystal oscillator if used (see section 10).

22 Power Supply Connections

The NJ1006A requires two power supplies. If the integrated antenna detector is used, a third power supply may be connected to the NJ1006A and is used to power the antenna. The recommended ranges are shown in Table 4. Power supplies need not to be regulated, but must be well filtered. This applies in particular to the analog power supply AVDD. TVDD may be taken from the GPS base-band processor board but should be sufficiently clean. If required, an RC or LC filter may be used.

Table 4: Power Supply

Power Supply	Min	Max
AVDD (Analog VDD)	2.2V	3.6V
TVDD (Digital VDD)	1.6V	AVDD+0.2V
PVDD (Antenna VDD)	2.2V	3.6V

No particular sequencing is needed while applying power to the NJ1006A. AVDD, PVDD and TVDD may be applied simultaneously or in any order.

Increasing TVDD above its maximum operating level (AVDD+0.2V) is not recommended. This will not cause any permanent damage, but the NJ1006A will not operate correctly. A battery 2.4V-3.0V may be used to supply AVDD if the battery load is kept reasonably constant. Sudden voltage variations as caused by a sudden load variation will disturb operation of the NJ1006A.

Good power supply decoupling is always required. A 100nF ceramic capacitor (X7R) mounted very close to the chip is recommended on AVDD, PVDD and TVDD. A 2.2μF (or higher) tantalum capacitor may be required on AVDD, especially if AVDD is not regulated.

23 PCB Layout Recommendations

The NJ1006A is a sensitive receiver. Although the IC is rather robust and easy to use, an improper PCB layout may degrade its performance significantly.

The best performance is generally achieved when the NJ1006A is placed over a solid ground plane with as little interruptions as possible. If a 2 layer PCB is used, the best

layout would be to use the bottom layer as ground plane with all routing made on the top layer.

A similar layout can be used also in multilayer PCBs, where internal layers can be used as ground plane instead of the bottom layer. It is however recommended to leave some spacing (at least 0.3mm) between the top layer and the ground plane, as this reduces losses and stray capacitances. Using layer 2 as ground plane with layer 1 for the routing is not recommended, as this results in too little spacing for most PCB build-ups.

Standard PCB materials such as FR4 can be used. Special low-loss substrates are in most cases not required to achieve proper performance, and would give only moderate performance improvements.

Proper connections are also important if good performance is to be achieved. The RF connections to the antenna and SAW filter shall be made with 50Ω striplines (unless their length does not exceed a couple mm), while vias on all RF connections shall be avoided.

Decoupling capacitors - especially on AVDD and VB - shall be connected very close to the chip using traces as wide as possible, with the other side of the capacitor well grounded (2-3 vias). AVSS and TVSS shall be connected to the ground plane as close to the chip package as possible, while 9 via holes shall be placed under the exposed die attach pad (DAP).

In order to avoid interference to the receiver from digital switching noise all digital signals shall be routed away from sensitive analog connections while some shielding is recommended. Most sensitive are the antenna and the LNA, followed by IF filter and crystal oscillator. Application note AN-002 gives several recommendations on how to prevent interference and should be read before starting a PCB design.

To guarantee proper mounting of the IC, the PCB land pattern shown in Figure 11 shall be used. In particular the following requirements shall be adhered to:

- The PCB shall meet the solderability requirements of IPC/JEDEC J-STD-003A and shall be flat to within 0.1mm per cm .
- The PCB lands shall have a width of 0.25mm and shall be 0.1-0.2mm longer than the package pin in the outside direction in order to promote proper solder fillet formation. The length of the PCB lands may also be increased by 50μm in the inside direction to improve heel formation.
- Vias inside PCB lands shall be plugged and metallized on top to prevent solder from wicking through the via hole. Unplugged vias inside PCB lands are not allowed.
- Vias, connected to the analog ground plane, are required under the DAP. The recommended number is 9, spaced about 1.2-1.3mm and with a drill diameter of 0.3-0.4mm.

- The copper area under the DAP shall have the same size of the DAP and shall be solder mask defined. A solder mask overlap of the copper edge of at least 63.5μm is recommended.
- A solder mask with tight openings is recommended to ensure that some solder mask remains between the PCB lands.
- PCB layout examples can be found in the NB1042A datasheet.
PCB Gerber data is also available and can be used as recommended layout. To request them please contact Nemerix SA support team at support@nemerix.com.

24 Mounting Recommendations

The NJ1006A shall be mounted on the PCB by reflow soldering. Please follow these recommendations:

- Stainless steel stencils with a thickness of 125-150μm are recommended for solder paste application. For improved solder paste release the walls of the apertures should be tapered and the corners rounded.
- To avoid applying an excessive amount of paste, it is recommended that multiple stencil openings - summing up to about 40% of the total area - are placed under the DAP (see Figure 11). Applying too much paste may result in lifted packages and unsoldered pins.
- Pb-free solder paste shall be used. Sn/Ag/Cu alloys with a melting point of 217°C are recommended. A typical reflow temperature profile is shown in Figure 9. The recommendations given by the solder paste manufacturer should also be followed.

Typically, the area under the profile curve, bounded by the liquidus temperature, defines the quality of the solder joint. Too little area leads to cold solder joints, which are a reliability risk. Too much area could result in undesirable metallurgical issues, that could also be a reliability risk.

Mounting the NJ1006A with Pb-containing alloys such as the old Sn60%-Pb40% alloy is possible but is not recommended and deprecated. The user will need to run appropriate experiments to define reflow conditions and possible reliability issues if alloys other than Sn/Ag/Cu are desired.

After assembly the board shall be cleaned to remove solder flux residue. Solder flux residue between pads or on RF components may cause high leakages which may increase RF losses to an unacceptable level. Ultrasonic cleaning shall not be used since many parts - especially crystals, SAW filters and TCXO - may be damaged. No-clean solder flux may be used to minimize cleaning requirements.

Table 5: Classification Reflow Profile

Profile Feature	Pb-Free Assembly
Average Ramp Up Rate	3 °C/second max.
Preheat Temperature Min (T_{Smin}) Temperature Min (T_{Smax}) Time (t_{Smin} to t_{Smax})	150 °C 200 °C 60 to 180 s
Time maintained above T_L t_L	217 °C 60 to 150 s
Peak/Classification Temperature (T_P)	260 °C
Time within 5 °C of actual Peak Temperature T_P	20 to 40 s
Ramp-Down Rate	6 °C/second max.
Time 25°C to Peak Temperature	8 minutes max.

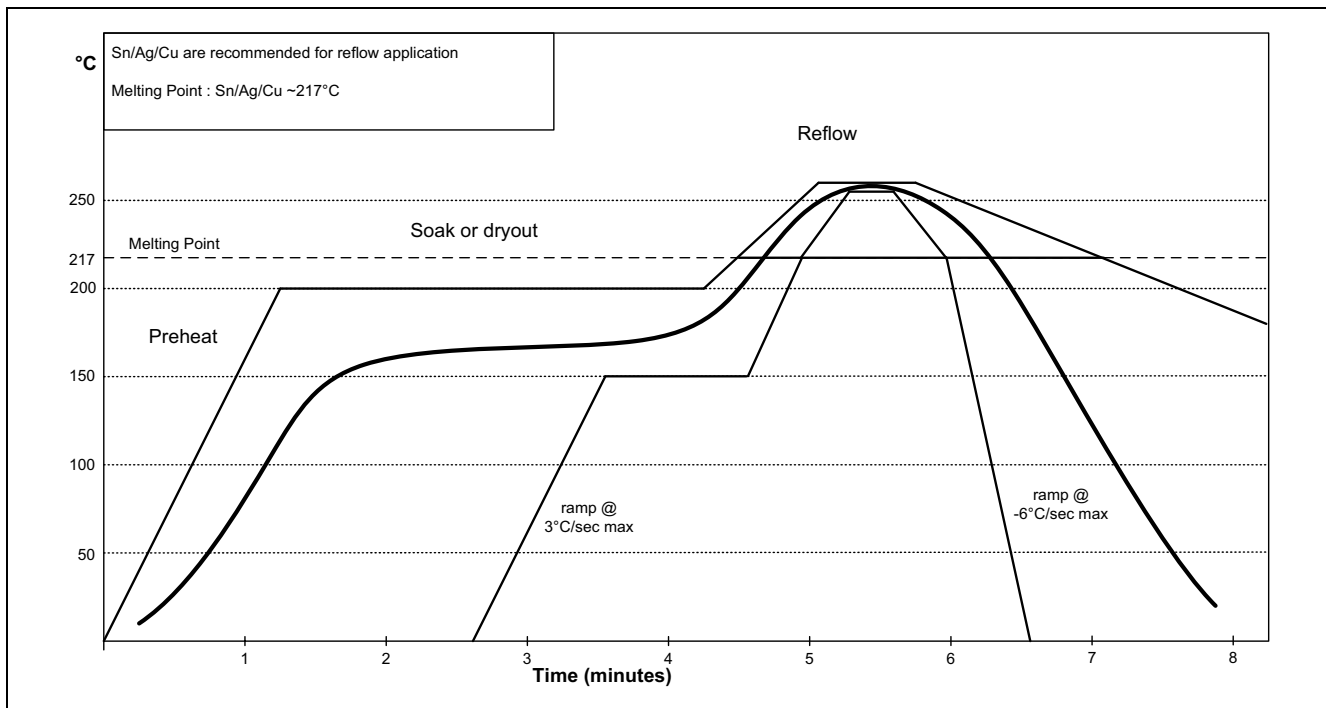


Figure 9: Recommended reflow profile for lead-free solder paste

25 Physical Dimensions

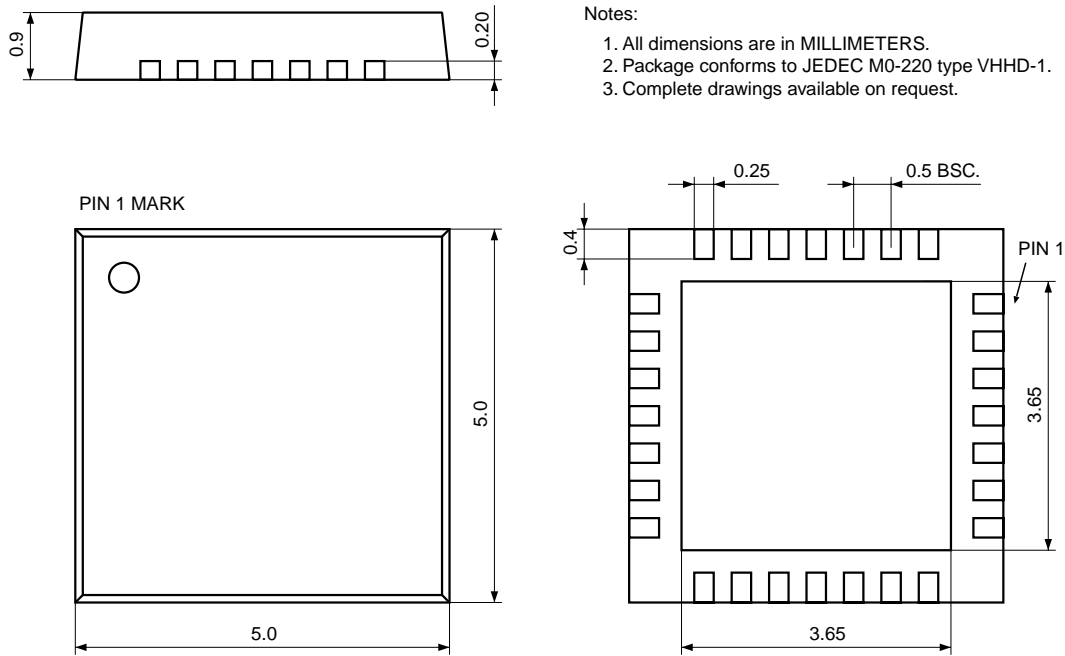


Figure 10. NJ1006AM, 28 Lead 5x5mm QFN Package

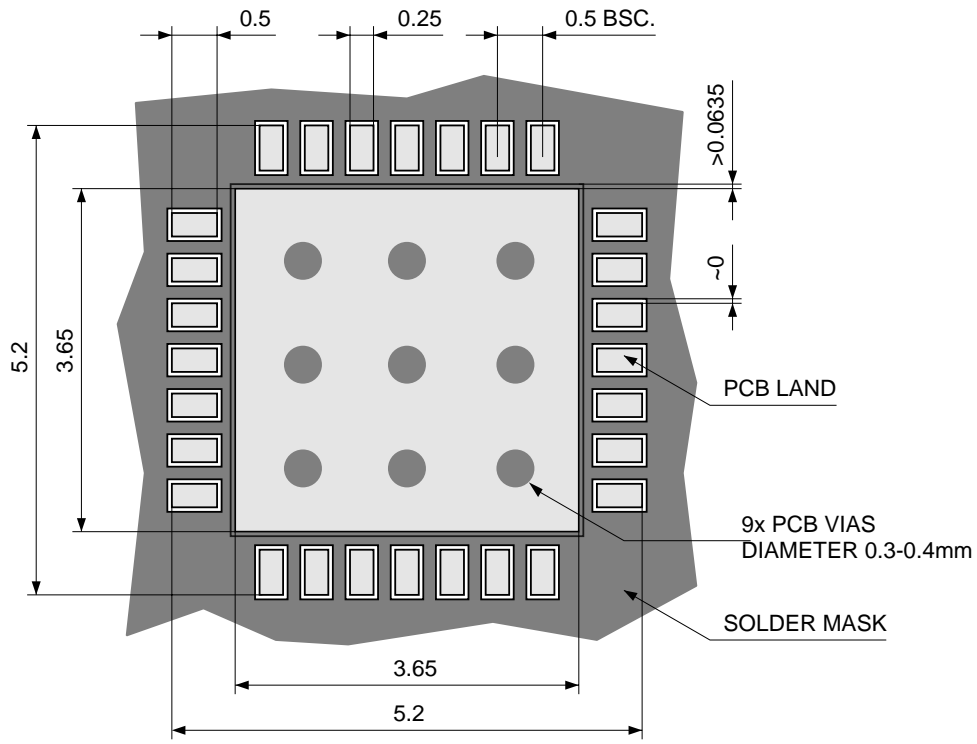


Figure 11. PCB land pattern, 5x5mm QFN package

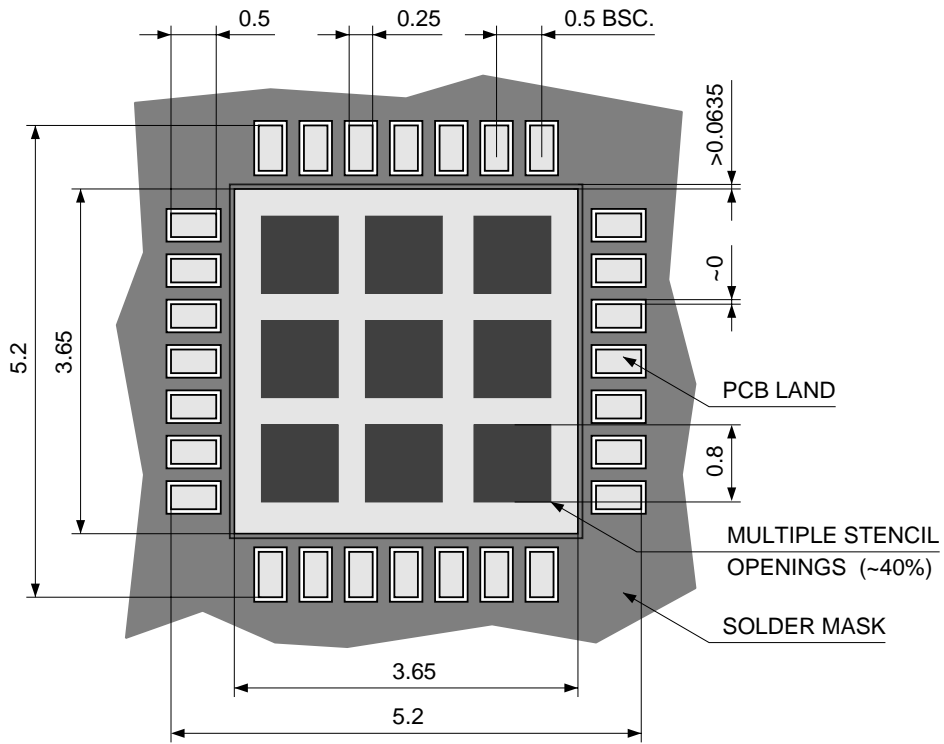


Figure 12. PCB solder paste stencil openings

Notes:

Ordering information

Part	Description
NJ1006AH	GPS Receiver RF Front-End IC 16.367 MHz and 13 MHz
NJ1006AI	GPS Receiver RF Front-End IC 19.x MHz
NJ1006AJ	GPS Receiver RF Front-End IC 12.6 MHz and 14.4 MHz
NJ1006AK	GPS Receiver RF Front-End IC 16.367 MHz and 15.36 MHz

Related products

Part	Description
EB1006A	Evaluation Board for NJ1006(A)
NJ1030A	GPS Baseband Processor
DK1030	NJ1030 Development Kit

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